

1.HSIC1_WLAN2SOC_DEVICE_RDY
2.PMU_GPIO_BT_REG_ON_R
3.PMU_GPIO_WLAN_REG_ON_R
4.PMU_GPIO_BT_REG_ON
5.PMU_GPIO_WLAN_REG_ON
6.JTAG_WLAN_TMS_TX_BLANK
7.JTAG_WLAN_TDI_OSCAR_A
8.HSIC1_SOC2WLAN_HOST_RDY_R
9.JTAG_WLAN_SEL
10.TP_JTAG_WLAN_TCK
11.TP_JTAG_WLAN_TRST_L
12.JTAG_WLAN_TDO_OSCAR_B
13.OSCAR2RADIO_CONTEXT_A
14.PMU_GPIO_WLAN_HOST_WAKE
15.VCC_MAIN_GRAPE_RAMP
16.WLAN_TX_BLANK
17.PP3V3_S2R
18.GPIO_BT_WAKE
19.SIM_TRAY_DETECT
20.UART2_SOC2WLAN_TX_R
21.SIMCRD_CLK_CONN_FILT
22.UART2_WLAN2SOC_TX_R

23.UART_BB2WLAN_LTE_COEX_R
24.UART_WLAN2BB_LTE_COEX_R
25.BOARD_TEMP3_P
26.SIMCRD_CLK_CONN

1.PMU_GPIO_CLK_32K_WLAN_R
2.UART1_BT2SOC_RTS_L
3.UART1_BT2SOC_TX
4.UART1_SOC2BT_RTS_L
5&12&15&17&21&26&28.GND
6.GPIO_SOC2GRAPE_RESET_L

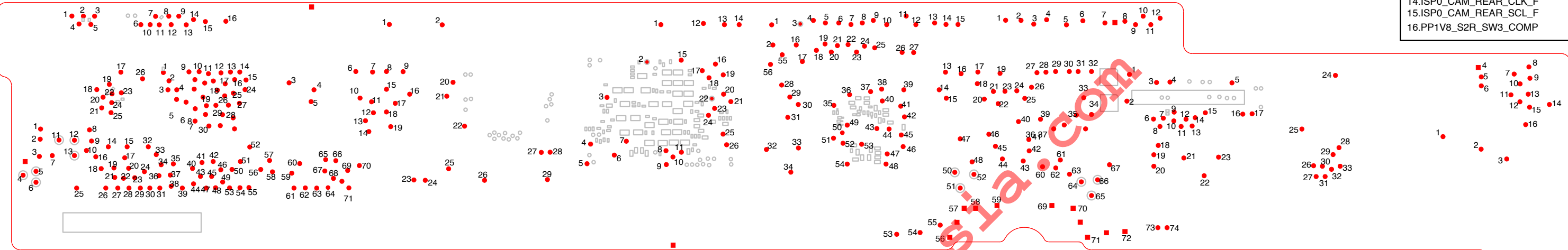
7.CUMULUS_M_VDDCORE
8.CUMULUS_M_VDDANA
9.CUMULUS_S_VDDCORE
10.TP_CUMULUS_S_H_SDO
11.TP_CUMULUS_S_H_SDI
13.CUMULUS_MS_CK
14.CUMULUS_S_BCFG_RTCK
16.JTAG_CUMULUS_S_TMS
18.CUMULUS_MS_SD
19.TP_CUMULUS_S_H_SCLK
20.CUMULUS_S_VDDANA
22.PP5V25_GRAPE

23.TP_CUMULUS_S_H_CS_L
24.GPIO_GRAPE2SOC_IRQ_L
25.PP1V8_GRAPE_SW
27.DISPLAY_SYNC
29.CUMULUS_M_BCFG_RTCK
30.SPI2_GRAPE_MOSI
31.TP_JTAG_CUMULUS_M_TDI
32.TP_JTAG_CUMULUS_M_TDO
33.SPI2_GRAPE_CS_L
34.TP_JTAG_CUMULUS_M_TCK
35.SPI2_GRAPE_SCLK
36.JTAG_CUMULUS_M_TMS

1&19&20&22&24&25&26&27&28&29&30&31&32&33.GND
2.PP1V8_SW1_FOREHEAD
3.PP_RF1_1V8_DIG
4.GPIO_SOC2BB_WAKE_MODEM
5.HSIC2_SOC2BB_HOST_RDY
6.PS_HOLD_PMIC
7.BB_JTAG_TMS
8.DEBUG_RST_L
9.USB_BB_DEBUG_N
10.USB_BB_DEBUG_P
11.BB_JTAG_TRST_L
12.BB_JTAG_TCK
13.BB_JTAG_TDI
14.BB_JTAG_TDO
15.BB_JTAG_RTCLK

16.PP_SMPS1_MSMC_1V05
17.PP_SMPS4_RF2_2V05
18.TP_BB_TEST_MODE_1
21.TP_BB_TEST_MODE_0
23.PP_SMPS2_RF1_1V3

1&2&4&5&6.GND
3.PP3V0_SENSOR_PROX_AD7149_FILT
7.PP2V9_AVDD_CAM_REAR_FILT
8.PP2V6_CAM_REAR_AF_FILT
9.CAM_REAR_VSYNC
10.PP1V8_CAM_REAR_FILT
11.ISP0_CAM_REAR_SHUTDOWN_L_F
12.ISP0_CAM_REAR_SDA_F
13.PP1V3_CAM_REAR_FILT
14.ISP0_CAM_REAR_CLK_F
15.ISP0_CAM_REAR_SCL_F
16.PP1V8_S2R_SW3_COMP



1.SIM_TRAY_DETECT_FILT
2.SIMCRD_RST_CONN_FILT
3.PP3V0_S2R_NAVAJ0_FILT
4&5&6.PPVBUS_E75_USB_CONN
7.PMU_GPIO_MB_HALL1_IRQ
8.SIMCRD_IO_CONN_FILT
9.PP_LDO6_RUIM_1V8_FILT
10.PMU_GPIO_MB_HALL2_IRQ_FILT
11&12&13&14&60.GND
15.MAX983X4_L1_GAIN
16.PMU_GPIO_MB_HALL2_IRQ
17.SPKRAMP_L1_OUT_P
18.LEFT_CH_OUT_N
19.LEFT_CH_OUT_P
20.SPKRAMP_L1_OUT_N
21.MAX983X4_L2_GAIN
22.AUD_SPKRAMP_MUTE_L
23.RIGHT_CH_OUT_N
24.RIGHT_CH_OUT_P
25.PP0UT_E75_ACC_ID1_CONN
26.SPKRAMP_L2_OUT_N
27.SPKRAMP_L2_OUT_P
28.PP0UT_E75_ACC_ID2_CONN
29.E75_DPAIR2_CONN_N
30.E75_DPAIR2_CONN_P
31.SPKRAMP_R2_OUT_P
32.MAX983X4_R1_GAIN
33.SPKRAMP_R1_OUT_P
34.SPKRAMP_R1_OUT_N
35.MAX983X4_R2_GAIN
36.SPKRAMP_R2_OUT_N
37.E75_ACC_DET_CONN_L

1.FMIO_CLE
2.BOARD_TEMP5_P
3.GPIO_BTN_HOME_L
4.PPVREF_FMI_NAND
5.PP1V8_EXT_SW
6.FMIO_RE_L
7.FMIO_CEO_L
8.FMIO_WE_L
9.FMIO_ALE
10.FMIO_AD<7>
11.FMIO_DQS
12.FMIO_AD<6>
13.FMIO_AD<5>
14.FMIO_AD<4>
15.FMIO_AD<0>
16.FMI1_AD<0>
17.FMIO_AD<1>
18.FMIO_AD<2>
19.FMIO_AD<3>
20.PP1V2_S2R
21.PP1V2_SW1
22.PP3V3_SW
23.I2C2_SDA_1V8
24.VCC_MAIN_PP3V3SW_RAMP
25.PP1V8_SW1
26.I2C2_SCL_1V8
27.JTAG_SOC_TDI
28.JTAG_SOC_SEL
29.UART6_TS_ACC_TXD

1.WDOG_SOC
2.SOC_TST_CLKOUT
3.PP1V2_SW1
4.JTAG_SOC_TRST_L
5.TP_JTAG_SOC_TDO
6.PPVREF_FMI_SOC
7&10&11&13&14.GND
8.HSIC1_WLAN2SOC_REMOTE_WAKE
9.UART6_TS_ACC_RXD
12.SOC_TESTMODE
15.UART1_SOC2BT_TX
16.TP_GPIO_DFU_STATUS
17.SPI2_GRAPE_MISO
18.SPI3_CODECS_L
19.GPIO_SOC2PMU_KEEPACT
20.UART0_SOC_TXD
21.WDOG_SOC2PMU_RESET_IN
22.SOC_TST_CPUSWITCH_OUT
23.PMU_GPIO_BT_HOST_WAKE
24.SOCHOT0_L
25.OSCAR_TIME_SYNC_HOST_INT
26.BOARD_TEMP7_P

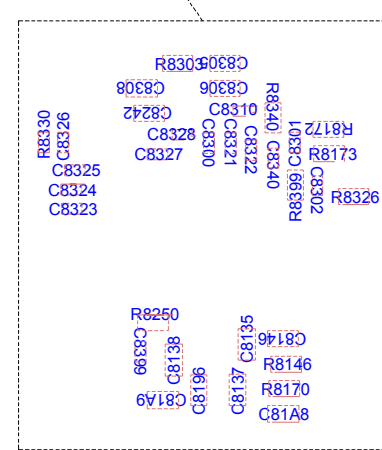
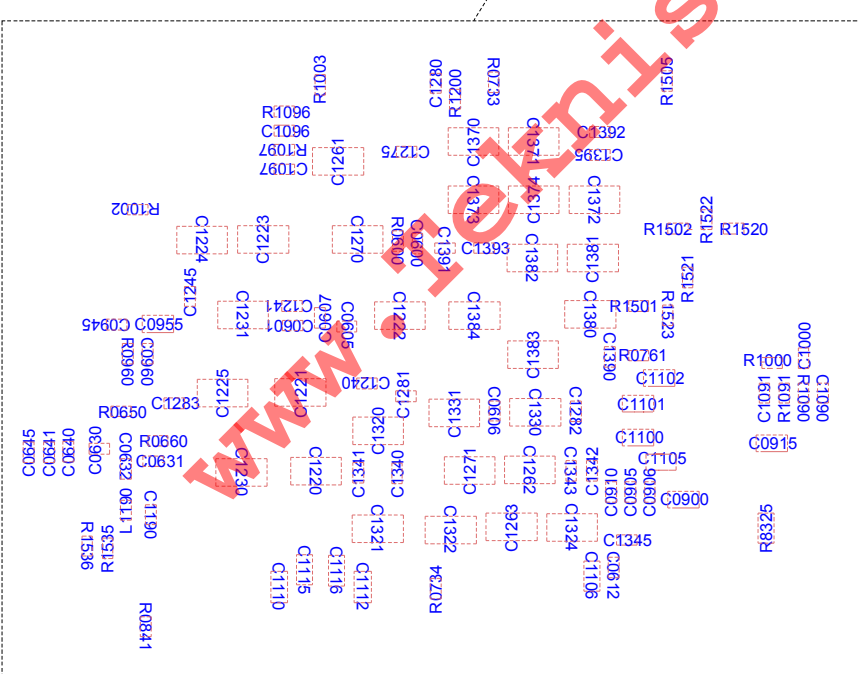
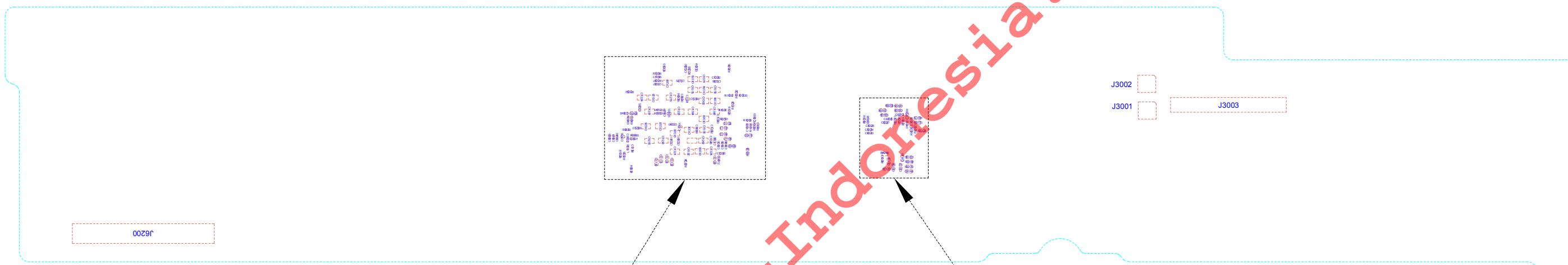
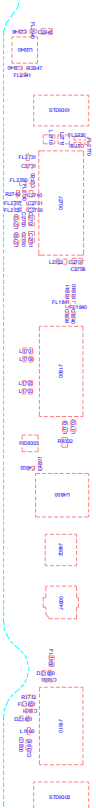
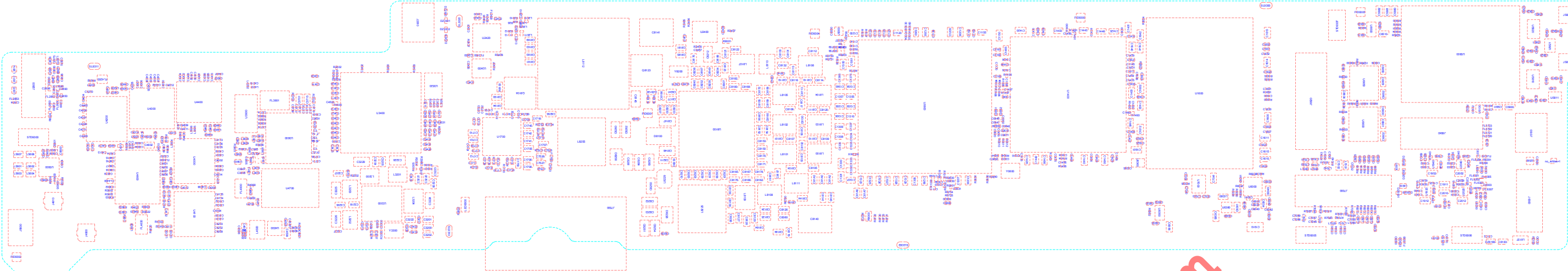
1.GPIO_TS2SOC2PMU_INT
2.SPI_OSCAR2COMPASS_CS_L
3.GPIO_FORCE_DFU
4.GPIO_SOC2BB_RST_L
5.PMU_GPIO_CLK_32K_OSCAR
6.GPIO_SOC2OSCAR_DBGEN
7.TP_OSCAR_P0_22
8.UART4_SOC2OSCAR_TXD
9.SPI_OSCAR_MISO
10.GPIO_SOC2OSCAR_DBGEN_R
11.PP3V0_S2R_SENSOR
12.PP1V2_S2R_SW2
13.GPIO_BB2SOC_GPS_SYNC
14.OSCAR2RADIO_CONTEXT_B
15.PP1V8_S2R_SW3
16.SOCHOT0_R_L
17.PPVDD_SRAM
18.PP3V0_UVLO
19.PMU_GPIO_OSCAR2PMU_HOST_WAKE
20.PMU_SHDWN
21.PP3V0_S2R_NAVAJ0
22.UART4_OSCAR2SOC_RXD
23.PPVDD_SOC
24.ACCEL2OSCAR_INT1
25.GPIO_OSCAR_RESET_L
26.PP2V9_CAM
27.PPVBUS_USB_DCIN
28.PPVDD_GPU
29.DWL_AP_CLK
30.SOCHOT1_L
31.PPVDD_CPU
32.PP1V0_SOC
33.USB_VBUS_DETECT
34.PP1V8_ALWAYS
35.BOARD_TEMP2_P
36.GPIO_PMU2SOC_IRQ_L
37.PP3V0_S2R_TRISTAR
38.PP2V6_CAM_AF
39.VBUS_PROT_G
40.PMU_TCAL
41.PP3V0_ALS
42.PMU_GPIO_PMU2BBPMU_RST_L
43.PPVBUS_PROT
44.BOARD_TEMP8_P
45.PMU_VCENTER
46.BOARD_TEMP6_P
47.TP_HV_CHG_EN
48.PPVCC_MAIN
49.TP_AMUX_B3
50.TP_AMUX_BY
51.TP_AMUX_AY
52.TP_AMUX_A3
53.PP1V8_SW1
54.PP1V8_SW2
55.I2C0_SCL_1V8
56.I2C0_SDA_1V8

1.GPIO_SOC2BB_WAKE_MODEM
2.GPIO_BTN_VOL_UP_L
3.GYRO2OSCAR_INT2
4.GPIO_BTN_VOL_DOWN_L
5.GPIO_BTN_SRL_L_FILT
6.PP3V0_GYRO
7.SPI_OSCAR2GYRO_CS_L
8.GPIO_BTN_VOL_UP_L_FILT
9.SIMCRD_IO_CONN
10.SIMCRD_RST_CONN
11.GPIO_BTN_ONOFF_L_FILT
12.GPIO_BTN_VOL_DOWN_L_FILT
13.GPIO_HS4_SHUNT_EN
14.PP3V0_SPARE1
15.PP6V0_LCM_VBOOST
16.GPIO_BB2SOC_RESET_DET_L
17.UART_WLAN2BB_LTE_COEX
18&58.BATT_NTC
19.GPIO_SOC2BB_RADIO_ON_L
20.GPIO_BTN_SRL_L
21.GPIO_BTN_ONOFF_L
22.PA_NTC_P
23.PP_LDO6_RUIM_1V8
24.GPIO_CODECS2SOC_IRQ_L
25.SPI3_CODECS_MISO
26.SPI3_CODECS_SCLK
27.GPIO_BB2SOC_GSM_TXBURST
28.ACCEL2OSCAR_INT2
29.GYRO2OSCAR_INT1
30.GYRO_DEN
31.SPI_OSCAR2ACCEL_CS_L
32.PP3V0_ACCEL
33.PPBATT_POS_RC
34.AIN3P
35.DMIC1_FF_SCLK
36.AIN3N
37.SPI3_CODECS_MOSI
38.PMU_GPIO_CODECS_HS_INT_L
39.L81_SPEAKER_VQ
40.GND
41.GND_AUDIO_CODECS
42&64&65&66&69.PPBATT_VCC
43&57.BATT_SWI_CONN
44.PMU_GPIO_BB_VBUS_DET
45.PMU_GPIO_BB2PMU_HOST_WAKE
46.PP1V8_S2R
47.PPLED_OUT_B
48.COMPASS2OSCAR_INT
50&51&52&55&58&59&71&72.GND
53.UART_BB2WLAN_LTE_COEX
54.MIKEY_TS_P
55.MIKEY_TS_N

1.PP3V0_COMP
2.PP3V0_S2R_SENSOR
3.SPI_OSCAR_SCLK
4.SPI_OSCAR_MOSI
5.PP1V8_COMP
6.I2C0_CAM_ALS_SCL_1V8_F
7.GPIO_CAM_ALS2SOC_IRQ_L_F
8.ISP1_CAM_FRONT_SDA_F
9.ISP1_CAM_FRONT_SCL_F
10.PP3V0_ALS_FILT
11.I2C0_CAM_ALS_SDA_1V8_F
12.ISP1_CAM_FRONT_CLK_F
13.ISP1_CAM_FRONT_SHUTDOWN_L_F
14.PP2V9_AVDD_CAM_FRONT_FILT
15.PP1V8_CAM_FRONT_FILT
16.GPIO_HS3_SHUNT_EN_FILT
17.CONN_HP_HEADSET_DET_FILT
18.GPIO_HS4_SHUNT_EN_FILT
19.CONN_HP_HS4_REF_FILT
20.CONN_HP_HS3_FILT
21.CONN_HP_RIGHT_FILT
22.CONN_HP_LEFT_FILT
23.CONN_HP_HS4_FILT
24.CONN_HP_HS3_REF_FILT
25.BOARD_TEMP4_P
26.DMIC1_FF_SCLK_FILT
27.DMIC1_FF_SD
28.DMIC1_FF_SD_FILT
29.PP1V8_DMIC_FILT
30.GPIO_HS3_SHUNT_EN

60.PP1V7_VA_VCP
61.PP1V7_VCP
62.L81_DMIC1_FF_SD
63.CODECS_HP_DET_R
67.GPIO_PROX2SOC_IRQ_L
70.BATT_SNS
73.PP_SMPS5_DSP_1V05
74.PP_LDO1





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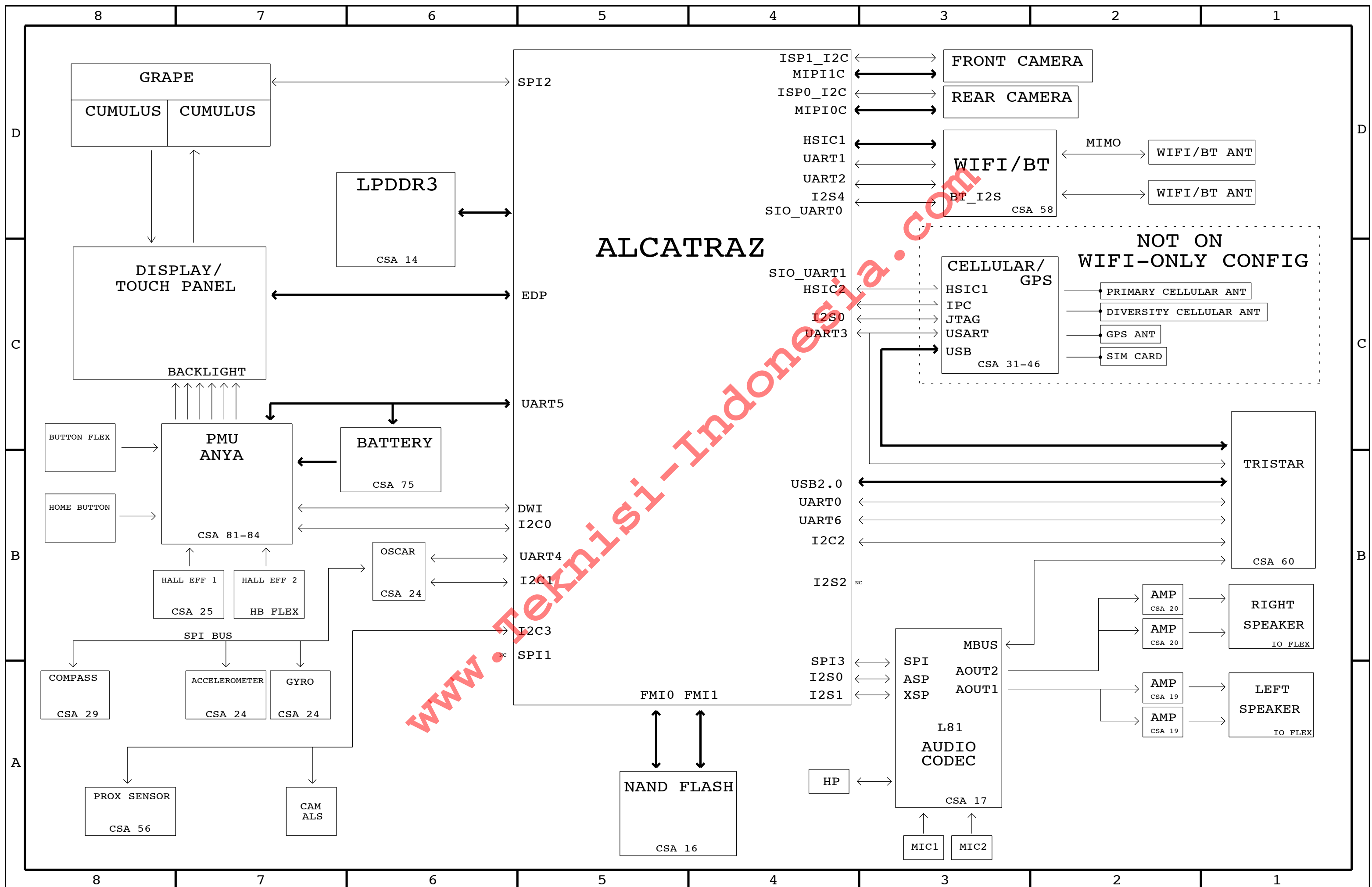
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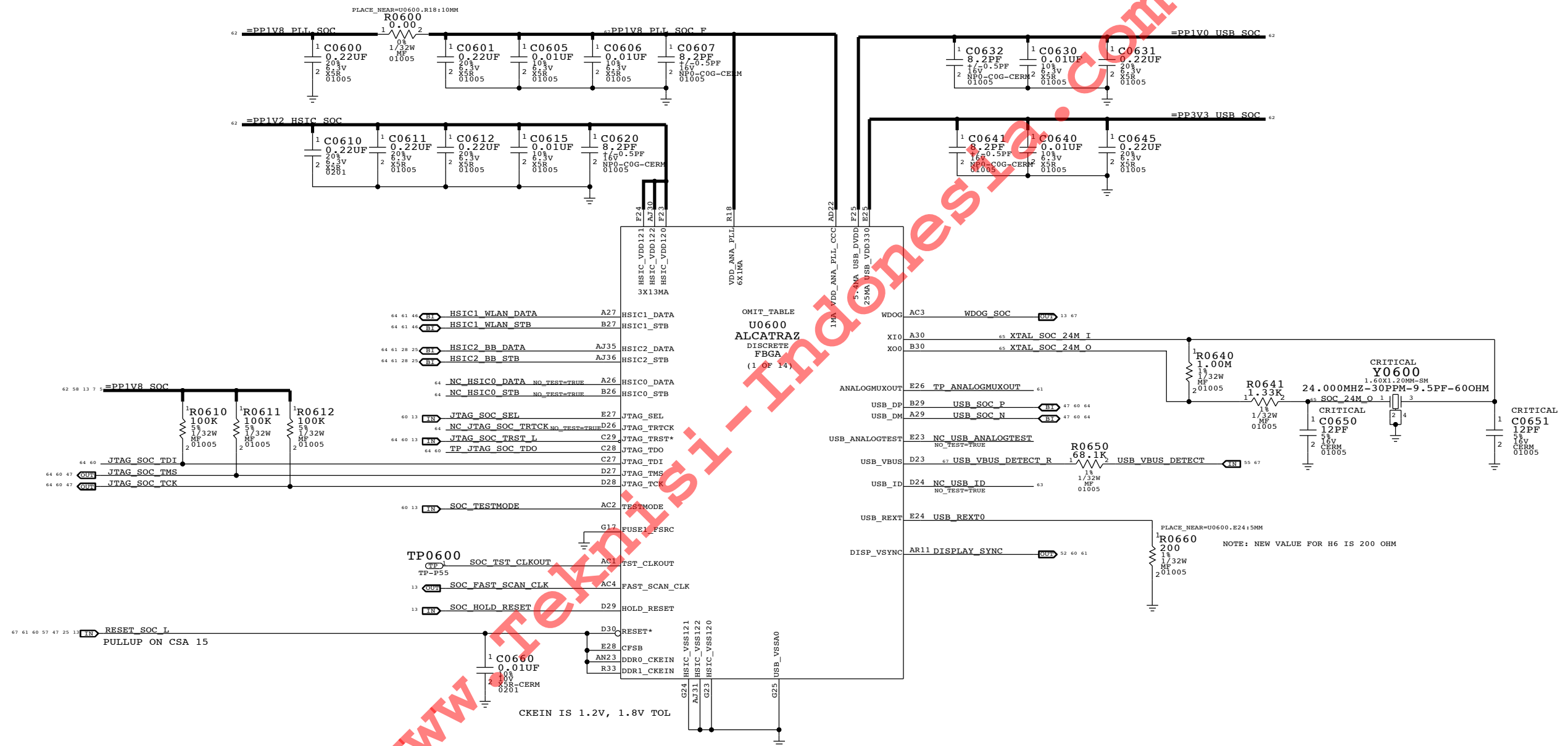
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2	2	BLOCK DIAGRAM: SYSTEM	N/A	N/A
3	4	BOM TABLES	N/A	N/A
4	6	SOC: MAIN	N/A	N/A
5	7	SOC: I/OS	N/A	N/A
6	8	SOC: NAND	N/A	N/A
7	9	SOC: DP,MIPI	N/A	N/A
8	10	SOC: DDR	N/A	N/A
9	11	SOC: IO POWER	N/A	N/A
10	12	SOC: SRAM POWER	N/A	N/A
11	13	SOC: CPU POWER	N/A	N/A
12	14	DDR: CHANNEL 0 AND 1	N/A	N/A
13	15	SOC: MISC & ALIASES	N/A	N/A
14	16	NAND: NAND	N/A	N/A
15	17	AUDIO: L81 CODEC	N/A	N/A
16	18	AUDIO: HP/DMIC FLEX CONNS	N/A	N/A
17	19	AUDIO: SPEAKER AMPS RIGHT	N/A	N/A
18	20	AUDIO: SPEAKER AMPS LEFT	N/A	N/A
19	24	SENSOR: OSCAR, GYRO, ACCEL	N/A	N/A
20	25	SENSOR: HALL EFFECT	N/A	N/A
21	26	IO: BUTTON FLEX CONN	N/A	N/A
22	27	CAMERA: FF AND ALS CONN	N/A	N/A
23	28	CAMERA: REAR CONN	N/A	N/A
24	29	SENSOR: COMPASS	N/A	N/A
25	30	CELL: SYSTEM & DEBUG CONNECTORS	RADIO_MLB_72_B7	06/03/2013

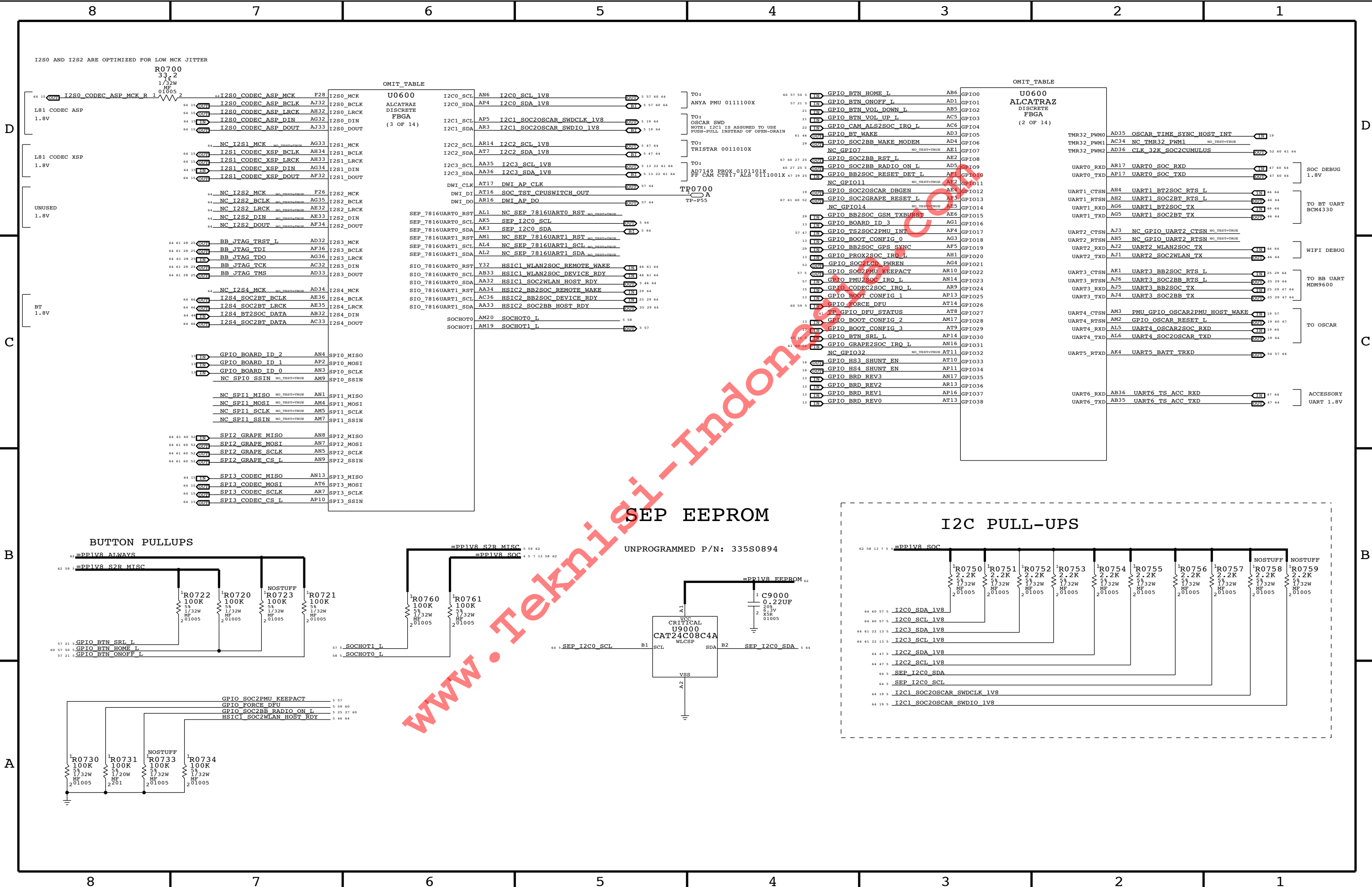
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27	33	CELL: BASEBAND PMU (2 OF 2)	RADIO_MLB_72_B7	06/03/2013
28	34	CELL: BASEBAND (1 OF 2)	RADIO_MLB_72_B7	06/03/2013
29	35	CELL: BASEBAND(2 OF 2)	RADIO_MLB_72_B7	06/03/2013
30	36	CELL: TRANSCEIVER (1 OF 2)	RADIO_MLB_72_B7	06/03/2013
31	37	CELL: TRANSCEIVER (2 OF 2)	RADIO_MLB_72_B7	06/03/2013
32	38	CELL: TRANSCEIVER MATCHING	RADIO_MLB_72_B7	06/03/2013
33	39	CELL: SAW BANK	RADIO_MLB_72_B7	06/03/2013
34	40	CELL: BAND 1/4 PAT	RADIO_MLB_72_B7	06/03/2013
35	41	CELL: BAND 2/3 PAD	RADIO_MLB_72_B7	06/03/2013
36	42	CELL: BAND 20 PAD	RADIO_MLB_72_B7	06/03/2013
37	43	CELL: BAND 5/8 PAD	RADIO_MLB_72_B7	06/03/2013
38	44	CELL: BAND 13/17 PAD	RADIO_MLB_72_B7	06/03/2013
39	45	CELL: PA DC/DC CONVERTER	RADIO_MLB_72_B7	06/03/2013
40	46	CELL: 2G FEM	RADIO_MLB_72_B7	06/03/2013
41	47	CELL: RX DIVERSITY	RADIO_MLB_72_B7	06/03/2013
42	48	CELL: GPS	RADIO_MLB_72_B7	06/03/2013
43	49	CELL: ANTENNA FEEDS	RADIO_MLB_72_B7	06/03/2013
44	51	CELL: SIM FLEX CONN	N/A	N/A
45	56	SENSOR: PROX AD7149	N/A	N/A
46	58	WIFI/BT: MODULE	WIFI_DEV	05/21/2013
47	60	IO: TRISTAR	N/A	N/A
48	61	IO: FILTERING	N/A	N/A
49	62	IO: FLEX HOTBAR PADS	N/A	N/A
50	63	IO: HOME BUTTON FILTERS	N/A	N/A

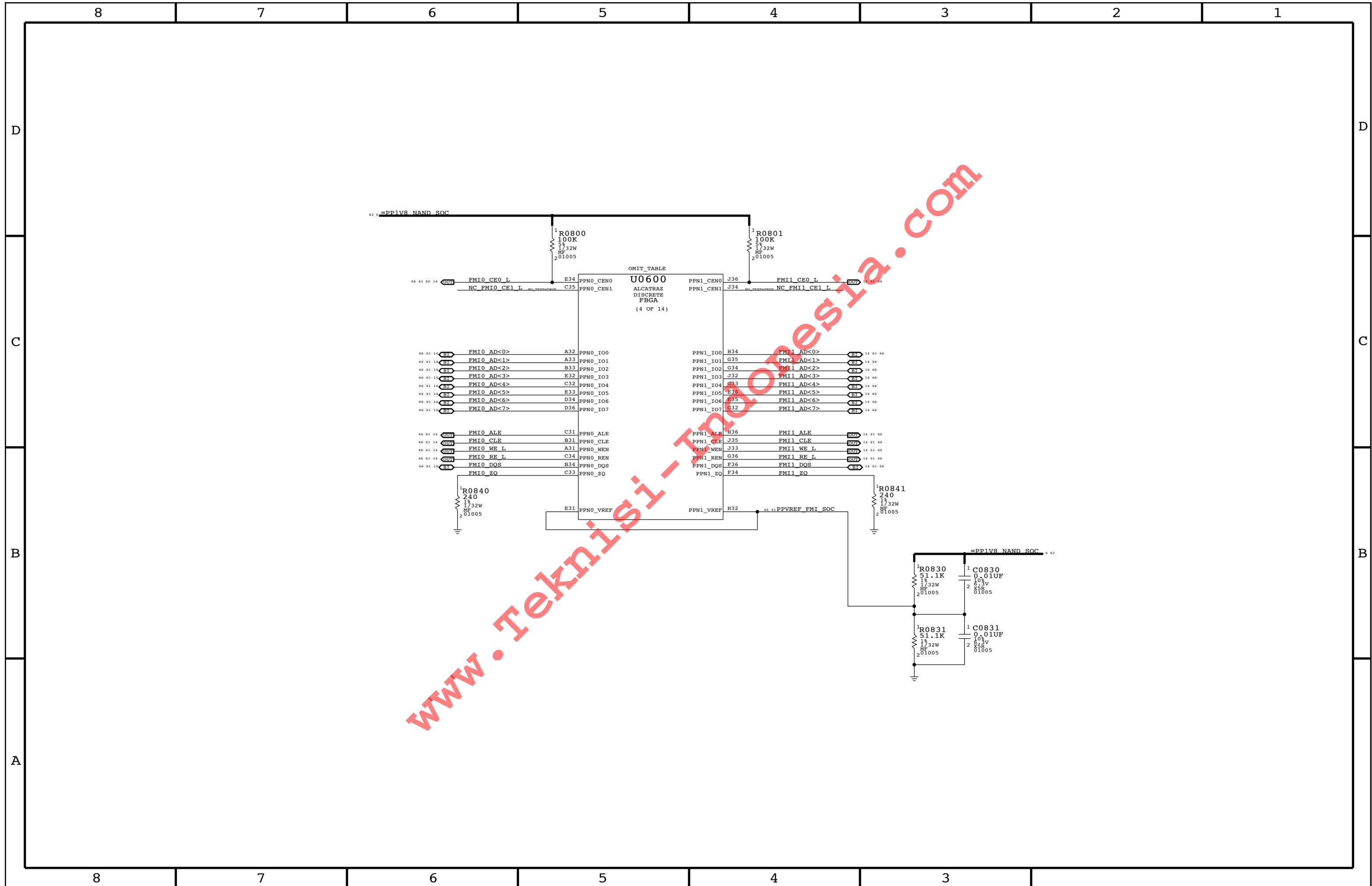
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52	66	GRAPE: CUMULUS	N/A	N/A
53	70	DISPLAY: EDP CONN	N/A	N/A
54	75	POWER: BATTERY CONNECTOR	N/A	N/A
55	81	PMU: ANYA PAGE 1	N/A	N/A
56	82	PMU: ANYA PAGE 2	N/A	N/A
57	83	PMU: ANYA PAGE 3	N/A	N/A
58	84	PMU: ANYA PAGE 4	N/A	N/A
59	90	SOC: DEBUG	N/A	N/A
60	93	TEST: TP/HOLES/FIDUCUALS	N/A	N/A
61	94	TEST: EE TP/PP	N/A	N/A
62	121	POWER: ALIASES	N/A	N/A
63	150	CONSTRAINTS: MLB RULES	N/A	N/A
64	151	CONSTRAINTS: LOW SPEED BUS	N/A	N/A
65	152	CONSTRAINTS: DISPLAY/AUDIO	N/A	N/A
66	153	CONSTRAINTS: DDR/FMI	N/A	N/A
67	154	CONSTRAINTS: POWER / GND	N/A	N/A
68	157	CONSTRAINTS: RF	N/A	N/A
69	158	CONSTRAINTS: WIFI/BT	WIFI_DEV	05/21/2013

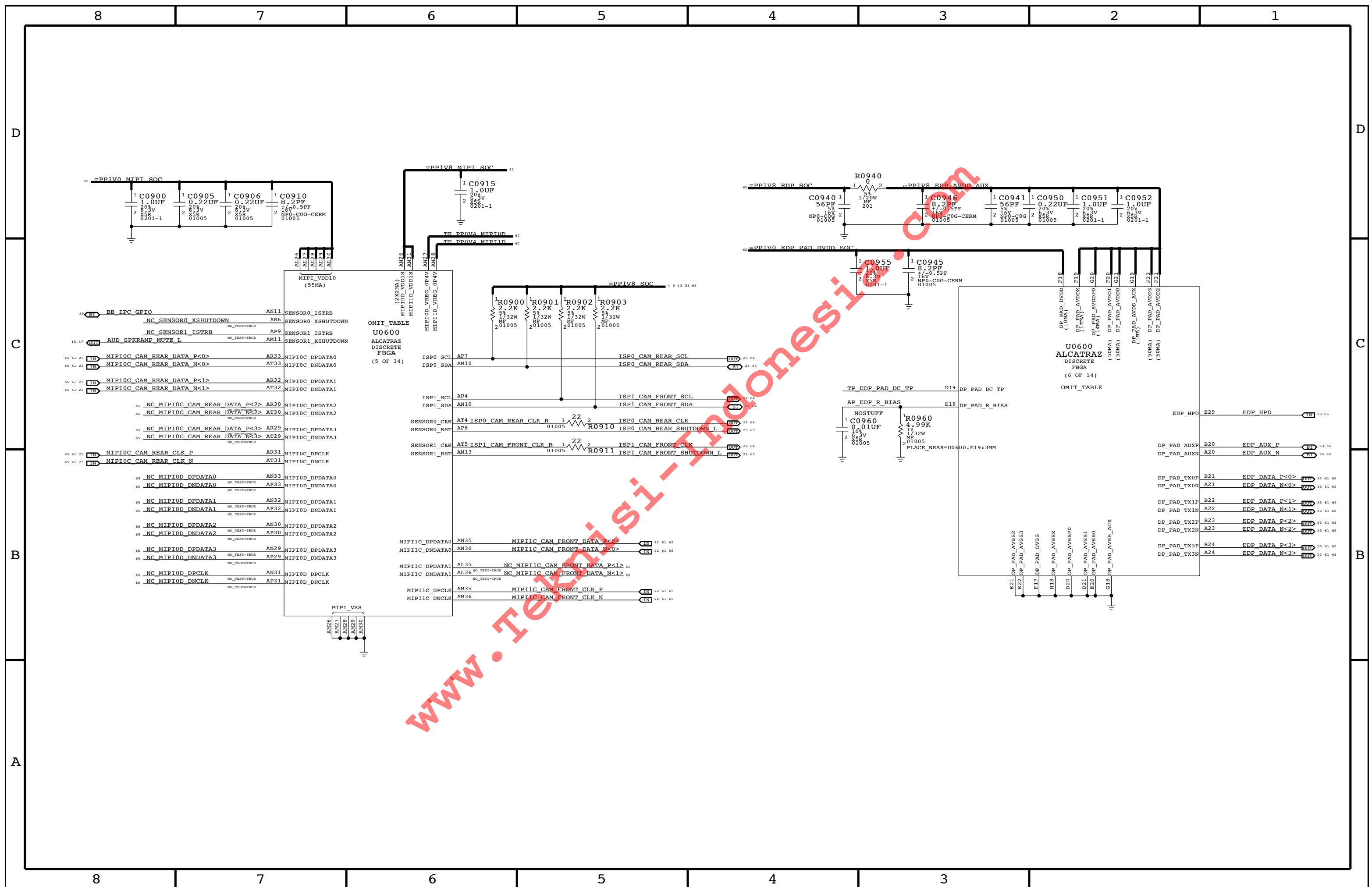
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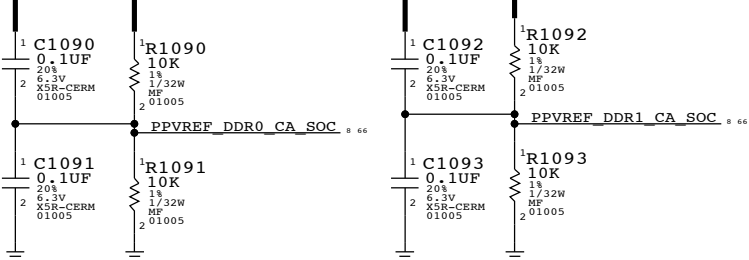
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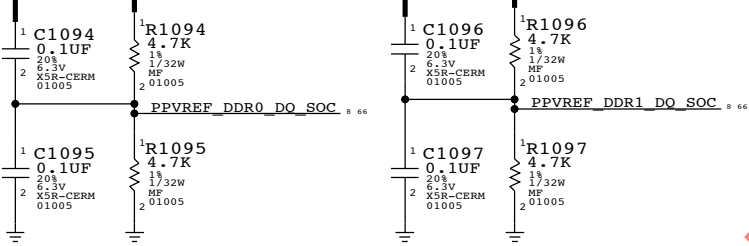
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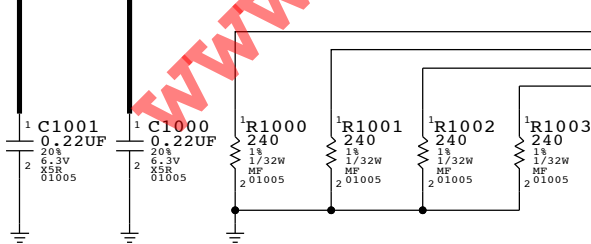
62 9 =PP1V2_S2R_DDR_SOC



62 9 =PP1V2_VDDIOD_SOC



62 9 =PP1V2_S2R_DDR_SOC



(DDR IMPEDANCE CONTROL)

OMIT TABLE

U0600
ALCATRAZ
DISCRETE
FBGA
(14 OF 14)

66 61 12	Q093	DDR0_CA<0>	AP27	DDR0_CA0
66 61 12	Q093	DDR0_CA<1>	AR27	DDR0_CA1
66 61 12	Q093	DDR0_CA<2>	AT27	DDR0_CA2
66 61 12	Q093	DDR0_CA<3>	AR26	DDR0_CA3
66 61 12	Q093	DDR0_CA<4>	AT26	DDR0_CA4
66 61 12	Q093	DDR0_CA<5>	AR20	DDR0_CA5
66 61 12	Q093	DDR0_CA<6>	AT20	DDR0_CA6
66 61 12	Q093	DDR0_CA<7>	AT19	DDR0_CA7
66 61 12	Q093	DDR0_CA<8>	AR19	DDR0_CA8
66 61 12	Q093	DDR0_CA<9>	AP19	DDR0_CA9

66 61 12	Q093	DDR0_CKE<0>	AR24	DDR0_CKE0
66 61 12	Q093	DDR0_CKE<1>	AT24	DDR0_CKE1
66 61 12	Q093	DDR0_CSN<0>	AR25	DDR0_CSN0
66 61 12	Q093	DDR0_CSN<1>	AT25	DDR0_CSN1

66 61 12	Q093	DDR0_DM<0>	D11	DDR0_DM0
66 61 12	Q093	DDR0_DM<1>	D9	DDR0_DM1
66 61 12	Q093	DDR0_DM<2>	C15	DDR0_DM2
66 61 12	Q093	DDR0_DM<3>	D7	DDR0_DM3

66 61 12	Q093	DDR0_DQ<0>	B15	DDR0_DQ0
66 61 12	Q093	DDR0_DQ<1>	D14	DDR0_DQ1
66 61 12	Q093	DDR0_DQ<2>	B14	DDR0_DQ2
66 61 12	Q093	DDR0_DQ<3>	D13	DDR0_DQ3
66 61 12	Q093	DDR0_DQ<4>	B13	DDR0_DQ4
66 61 12	Q093	DDR0_DQ<5>	D12	DDR0_DQ5
66 61 12	Q093	DDR0_DQ<6>	C12	DDR0_DQ6
66 61 12	Q093	DDR0_DQ<7>	B12	DDR0_DQ7
66 61 12	Q093	DDR0_DQ<8>	C11	DDR0_DQ8
66 61 12	Q093	DDR0_DQ<9>	B11	DDR0_DQ9
66 61 12	Q093	DDR0_DQ<10>	D10	DDR0_DQ10
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66 61 12	Q093	DDR0_DQ<13>	D8	DDR0_DQ13
66 61 12	Q093	DDR0_DQ<14>	C8	DDR0_DQ14
66 61 12	Q093	DDR0_DQ<15>	B8	DDR0_DQ15
66 61 12	Q093	DDR0_DQ<16>	D18	DDR0_DQ16
66 61 12	Q093	DDR0_DQ<17>	B18	DDR0_DQ17
66 61 12	Q093	DDR0_DQ<18>	D17	DDR0_DQ18
66 61 12	Q093	DDR0_DQ<19>	B17	DDR0_DQ19
66 61 12	Q093	DDR0_DQ<20>	D16	DDR0_DQ20
66 61 12	Q093	DDR0_DQ<21>	C16	DDR0_DQ21
66 61 12	Q093	DDR0_DQ<22>	B16	DDR0_DQ22
66 61 12	Q093	DDR0_DQ<23>	D15	DDR0_DQ23
66 61 12	Q093	DDR0_DQ<24>	C7	DDR0_DQ24
66 61 12	Q093	DDR0_DQ<25>	B7	DDR0_DQ25
66 61 12	Q093	DDR0_DQ<26>	D6	DDR0_DQ26
66 61 12	Q093	DDR0_DQ<27>	B6	DDR0_DQ27
66 61 12	Q093	DDR0_DQ<28>	D5	DDR0_DQ28
66 61 12	Q093	DDR0_DQ<29>	B5	DDR0_DQ29
66 61 12	Q093	DDR0_DQ<30>	D4	DDR0_DQ30
66 61 12	Q093	DDR0_DQ<31>	B4	DDR0_DQ31

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66 61 12	Q093	DDR0_DQS_P<1>	A9	DDR0_PDQS1
66 61 12	Q093	DDR0_DQS_P<2>	A18	DDR0_PDQS2
66 61 12	Q093	DDR0_DQS_P<3>	A5	DDR0_PDQS3

66 61 12	Q093	DDR0_DQS_N<0>	A13	DDR0_NDQS0
66 61 12	Q093	DDR0_DQS_N<1>	A10	DDR0_NDQS1
66 61 12	Q093	DDR0_DQS_N<2>	A17	DDR0_NDQS2
66 61 12	Q093	DDR0_DQS_N<3>	A6	DDR0_NDQS3

66 61 12	Q093	DDR0_CK_P	AT22	DDR0_CK
66 61 12	Q093	DDR0_CK_N	AR22	DDR0_CKB

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DDR1_CA1	L35	DDR1_CA<1>	Q093	12 61 66
DDR1_CA2	L36	DDR1_CA<2>	Q093	12 61 66
DDR1_CA3	M35	DDR1_CA<3>	Q093	12 61 66
DDR1_CA4	M36	DDR1_CA<4>	Q093	12 61 66
DDR1_CA5	V35	DDR1_CA<5>	Q093	12 61 66
DDR1_CA6	V36	DDR1_CA<6>	Q093	12 61 66
DDR1_CA7	W36	DDR1_CA<7>	Q093	12 61 66
DDR1_CA8	W35	DDR1_CA<8>	Q093	12 61 66
DDR1_CA9	W34	DDR1_CA<9>	Q093	12 61 66

DDR1_CKE0	F35	DDR1_CKE<0>	Q093	12 61 66
DDR1_CKE1	F36	DDR1_CKE<1>	Q093	12 61 66
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DDR1_DQ15	U2	DDR1_DQ<15>	Q093	12 61 66
DDR1_DQ16	G4	DDR1_DQ<16>	Q093	12 61 66
DDR1_DQ17	G2	DDR1_DQ<17>	Q093	12 61 66
DDR1_DQ18	H4	DDR1_DQ<18>	Q093	12 61 66
DDR1_DQ19	H2	DDR1_DQ<19>	Q093	12 61 66
DDR1_DQ20	J4	DDR1_DQ<20>	Q093	12 61 66
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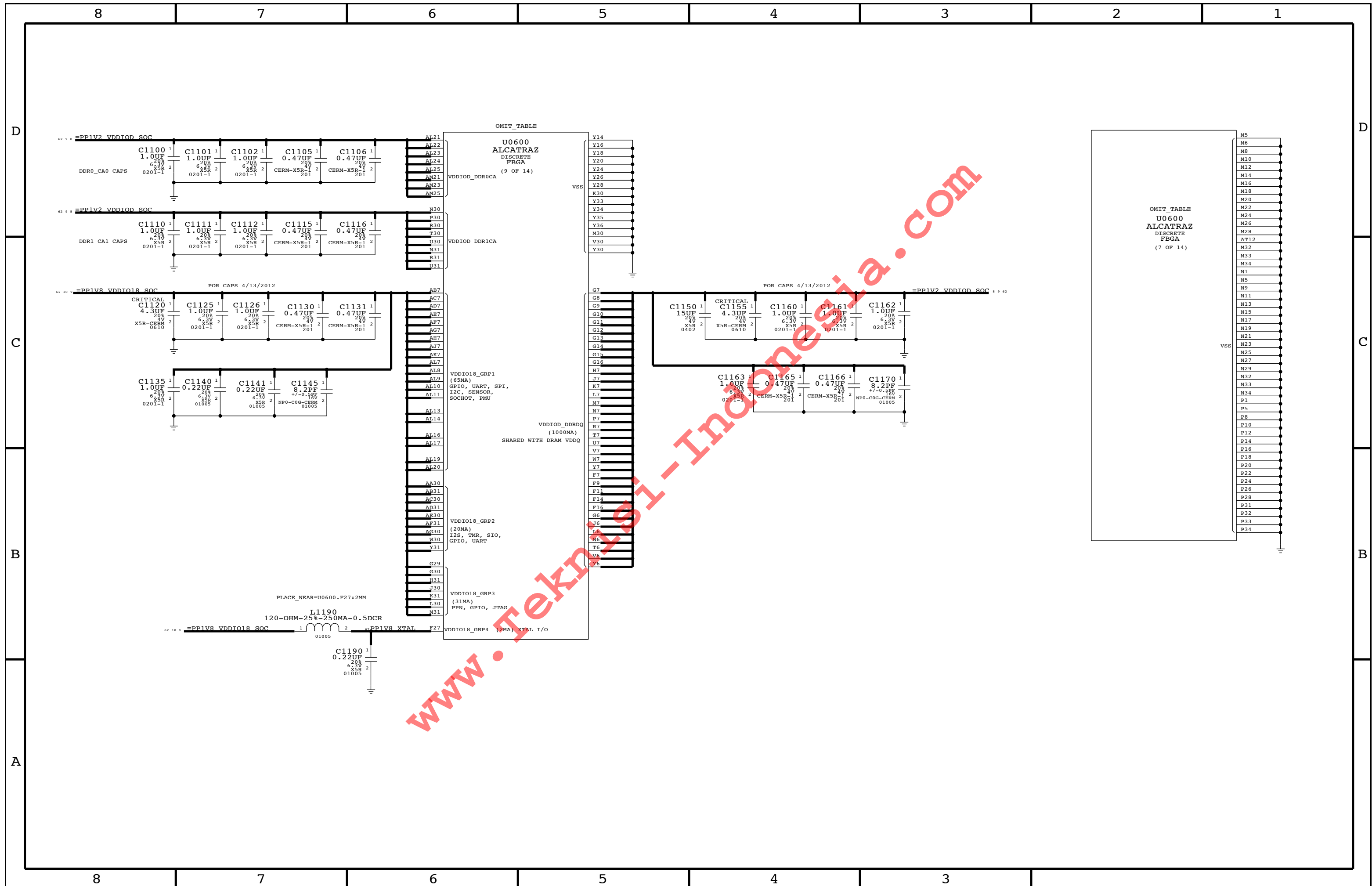
DDR1_PDQS0	L1	DDR1_DQS_P<0>	Q093	12 61 66
DDR1_PDQS1	T1	DDR1_DQS_P<1>	Q093	12 61 66
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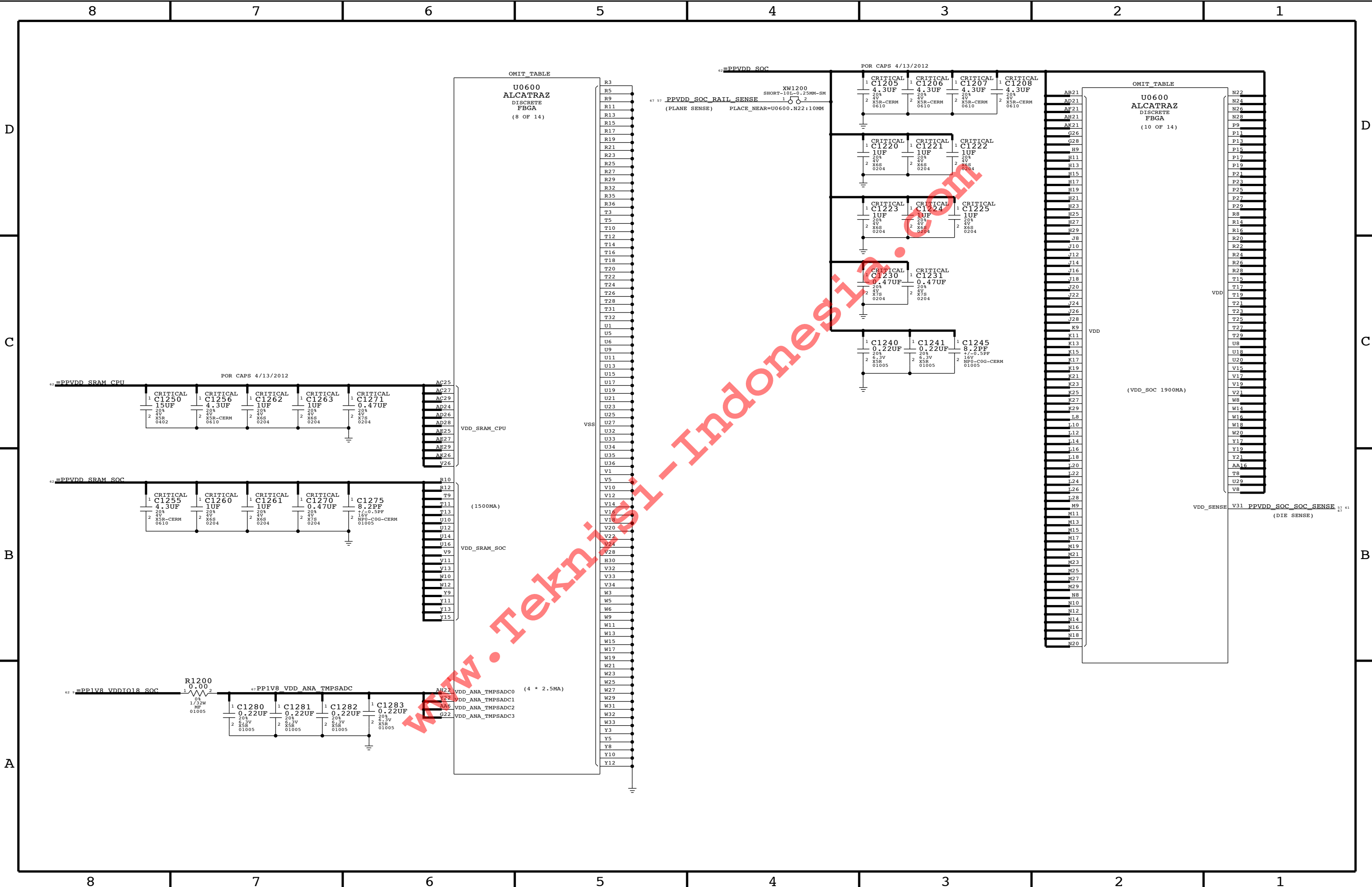
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DDR1_NDQS2	H1	DDR1_DQS_N<2>	Q093	12 61 66
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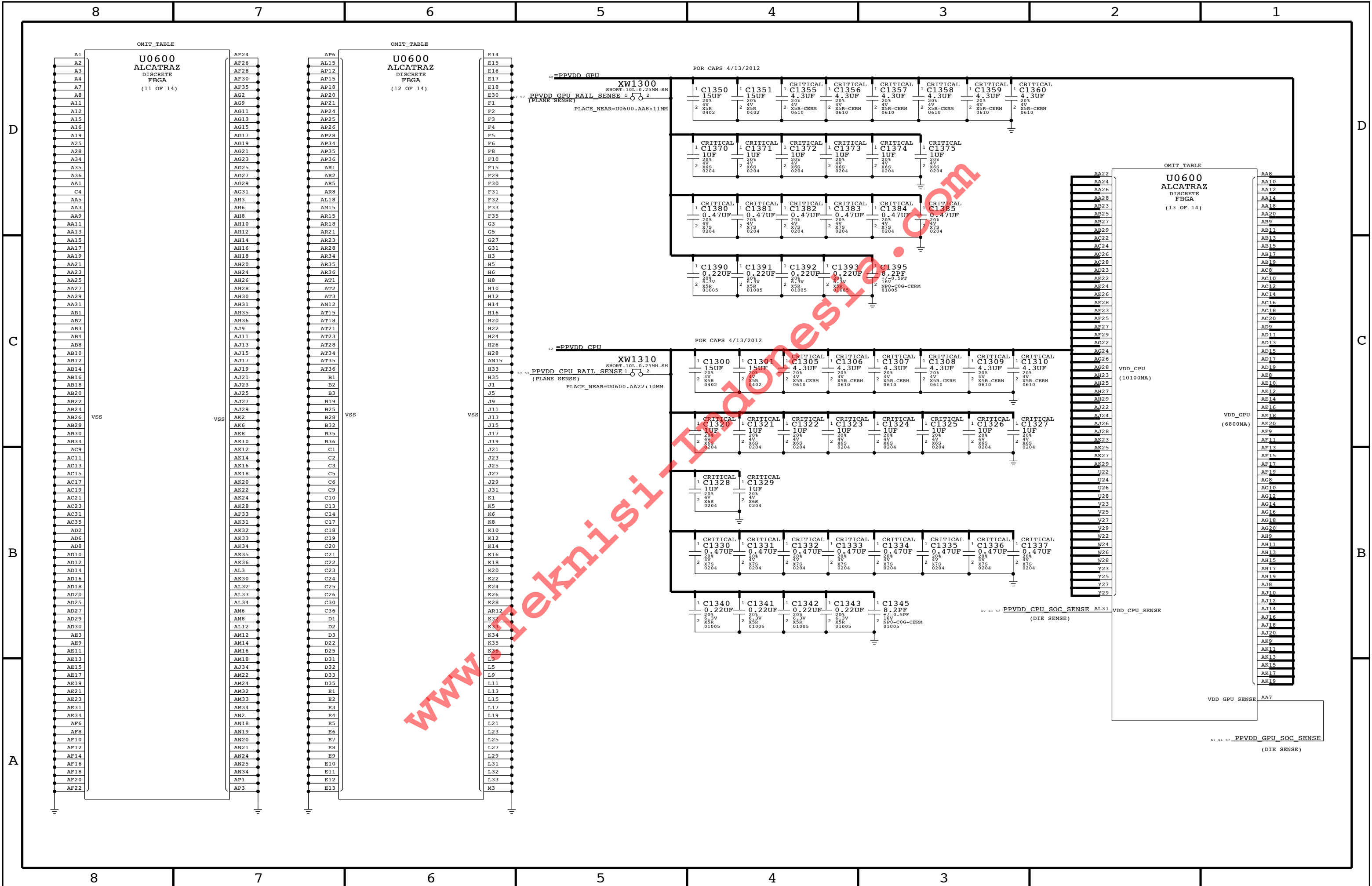
DDR1_CK	T36	DDR1_CK_P	Q093	12 61 66
DDR1_CKB	T35	DDR1_CK_N	Q093	12 61 66

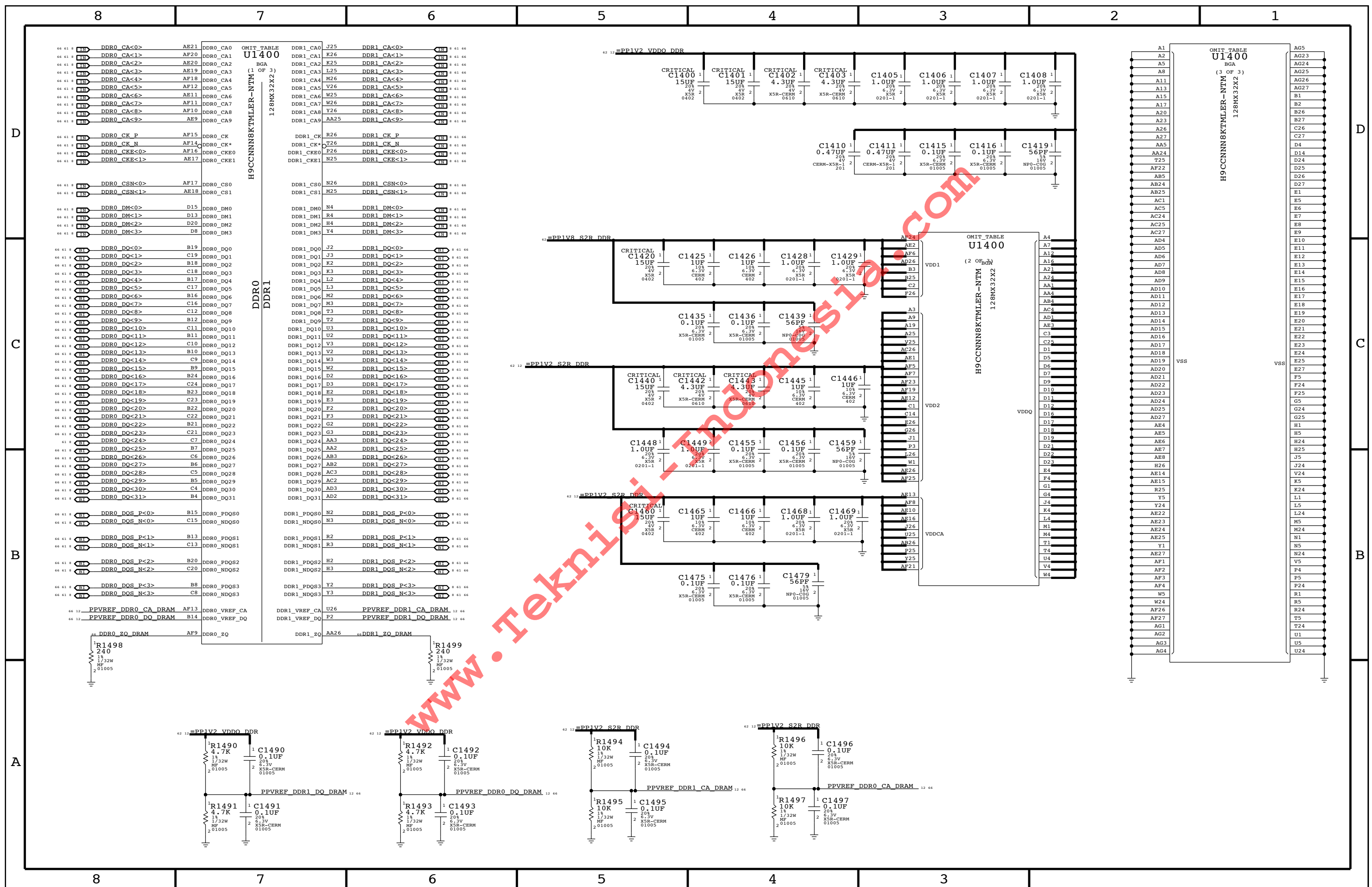
DDR0_VDD_CKE
DDR1_VDD_CKE (<1MA EACH)

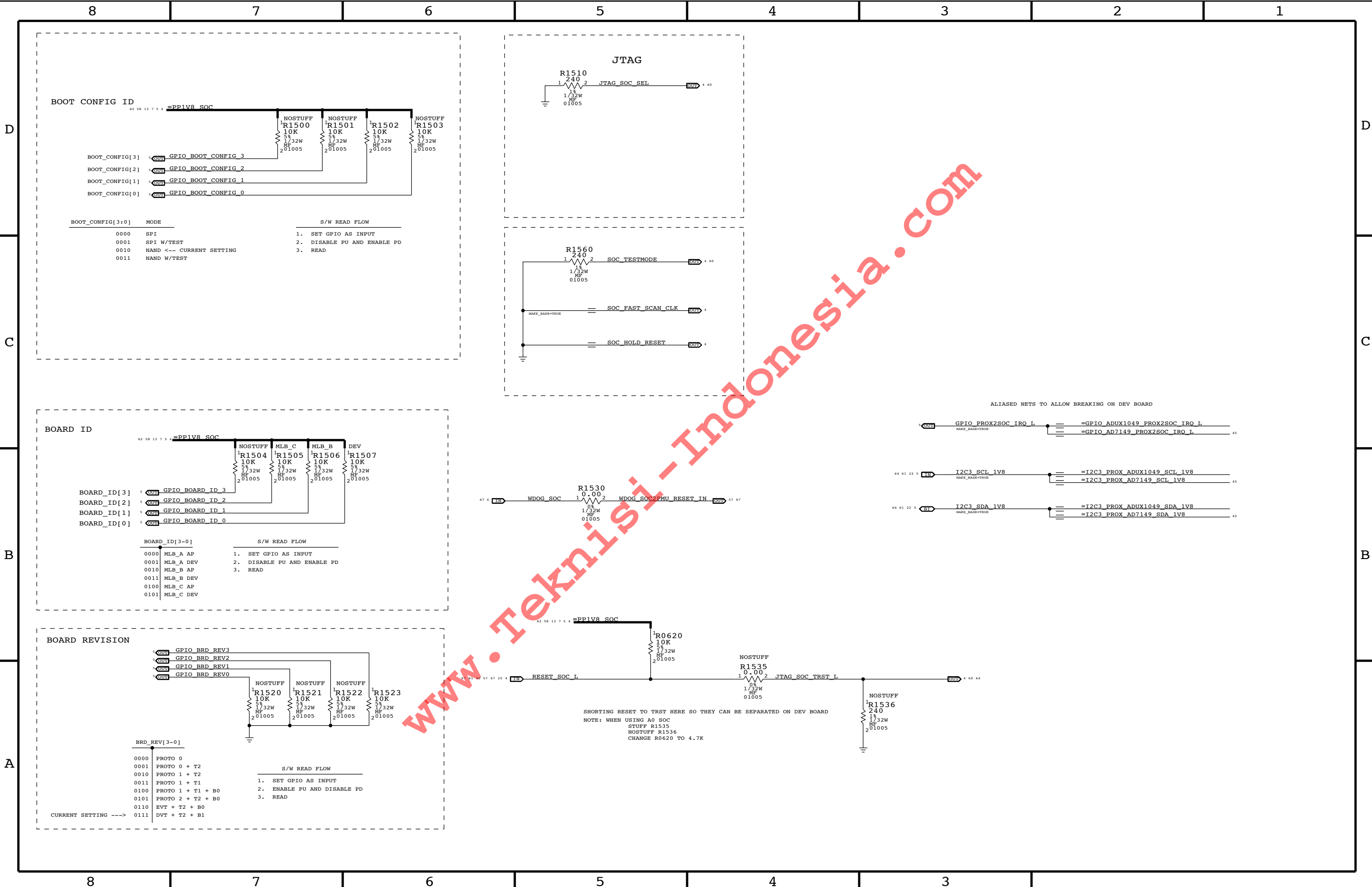
66	DDR0_CA_ZQ_SOC	AN22	DDR0_RREF_CA
66	DDR1_CA_ZQ_SOC	T33	DDR1_RREF_CA
66	DDR0_DQ_ZQ_SOC	F12	DDR0_RREF_DQ
66	DDR1_DQ_ZQ_SOC	R6	DDR1_RREF_DQ
66	PPVREF_DDR0_CA_SOC	AP22	DDR0_VREF_CA
66	PPVREF_DDR1_CA_SOC	T34	DDR1_VREF_CA
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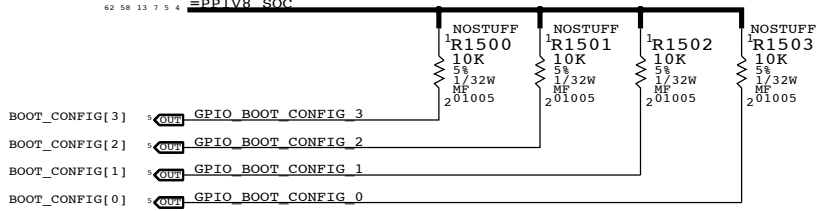






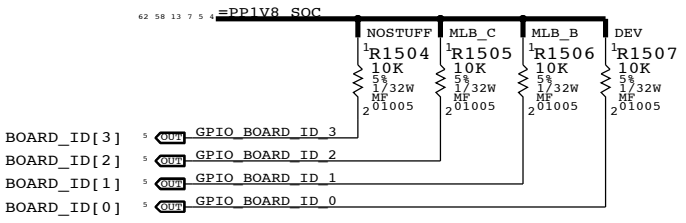


BOOT CONFIG ID



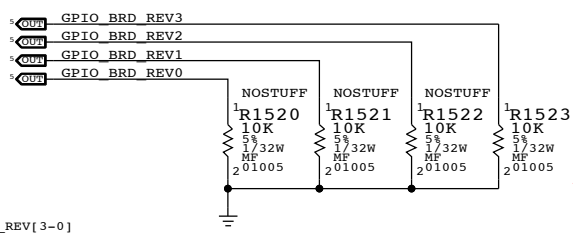
BOOT_CONFIG[3:0]	MODE	S/W READ FLOW
0000	SPI	1. SET GPIO AS INPUT
0001	SPI W/TEST	2. DISABLE PU AND ENABLE PD
0010	NAND <-- CURRENT SETTING	3. READ
0011	NAND W/TEST	

BOARD ID



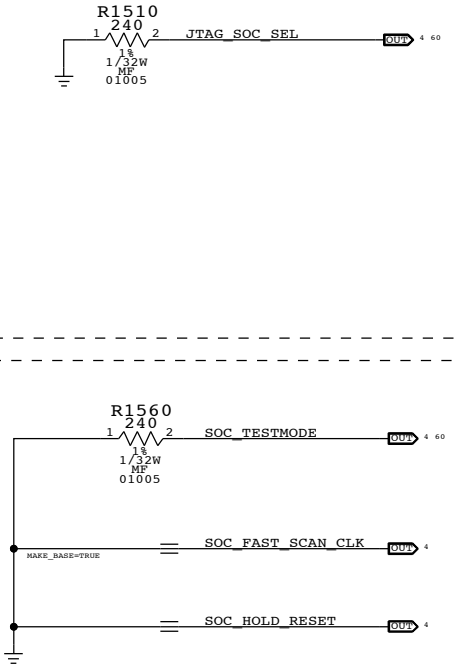
BOARD_ID[3-0]	S/W READ FLOW
0000	MLB_A AP
0001	MLB_A DEV
0010	MLB_B AP
0011	MLB_B DEV
0100	MLB_C AP
0101	MLB_C DEV

BOARD REVISION

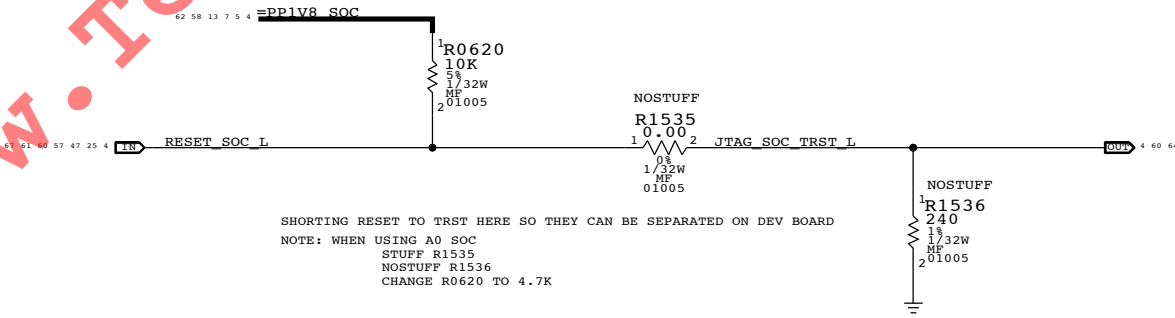
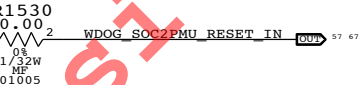
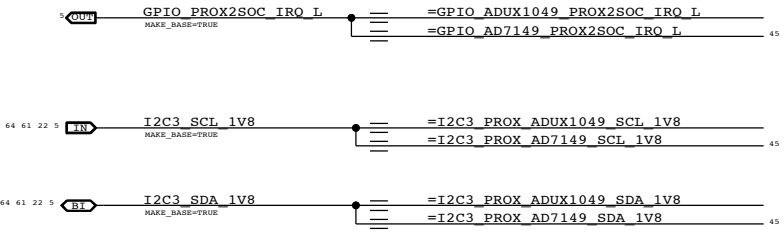


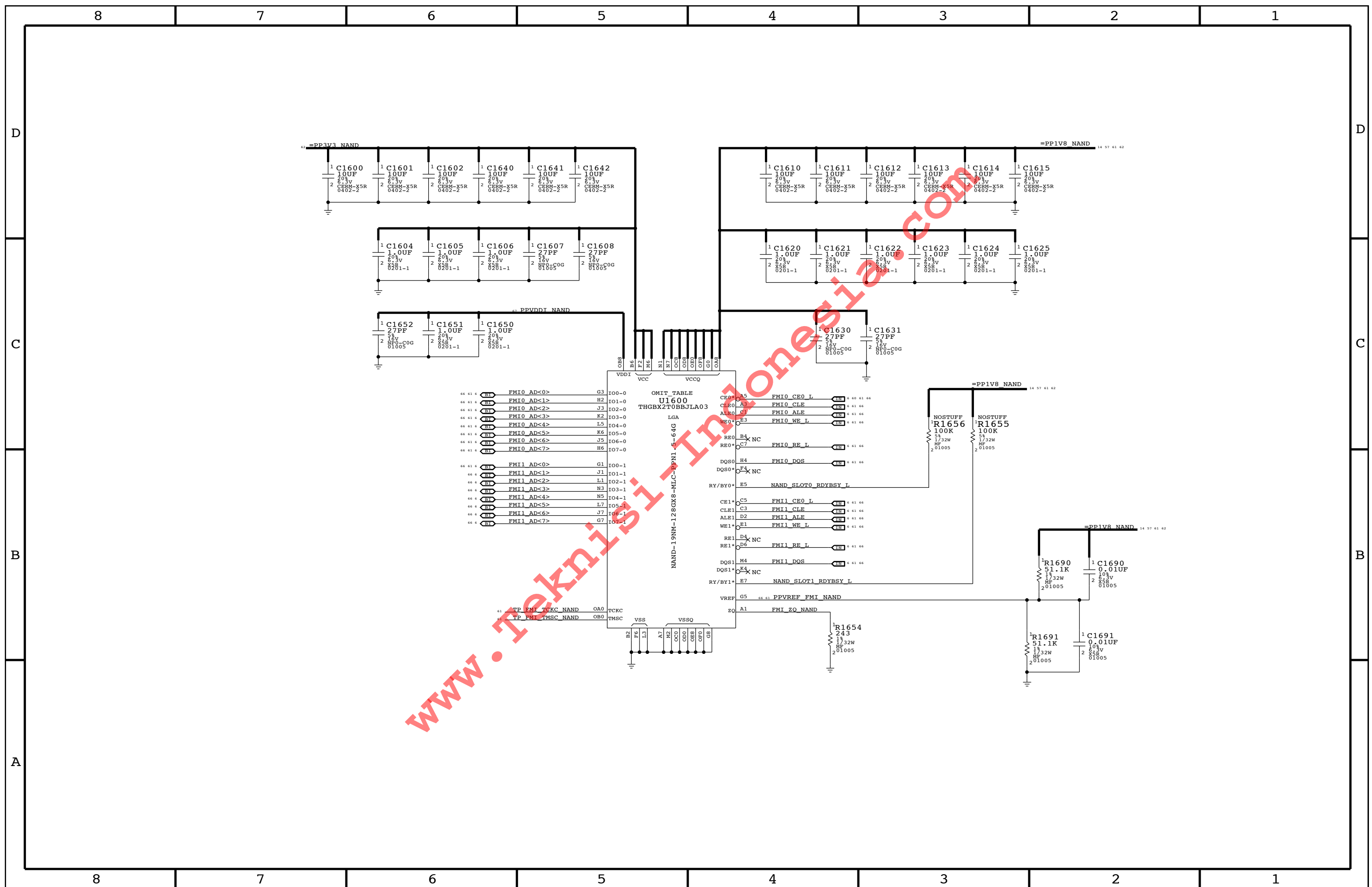
S/W READ FLOW
1. SET GPIO AS INPUT
2. ENABLE PU AND DISABLE PD
3. READ

JTAG



ALIASED NETS TO ALLOW BREAKING ON DEV BOARD





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SPEAKER AMPLIFIER

APN: 353S3445
TURN ON TIME: 3.5MS
TURN ON DELAY: ?MS
75HZ +/- XXX%

GAIN	VDD	GND
12DB	NC	SHORT
9DB	NC	100K
6DB	SHORT	NC
3DB	100K	NC
0DB	NC	NC

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APN: 353S3445
TURN ON TIME: 3.5MS
TURN ON DELAY: ?MS
75HZ +/- XXX%

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9DB	NC	100K
6DB	SHORT	NC
3DB	100K	NC
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www.Teknisi.com

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www.Teknisi.com

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3DB	100K	NC
0DB	NC	NC

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APN: 353S3445
TURN ON TIME: 3.5MS
TURN ON DELAY: ?MS
75HZ +/- XXX%

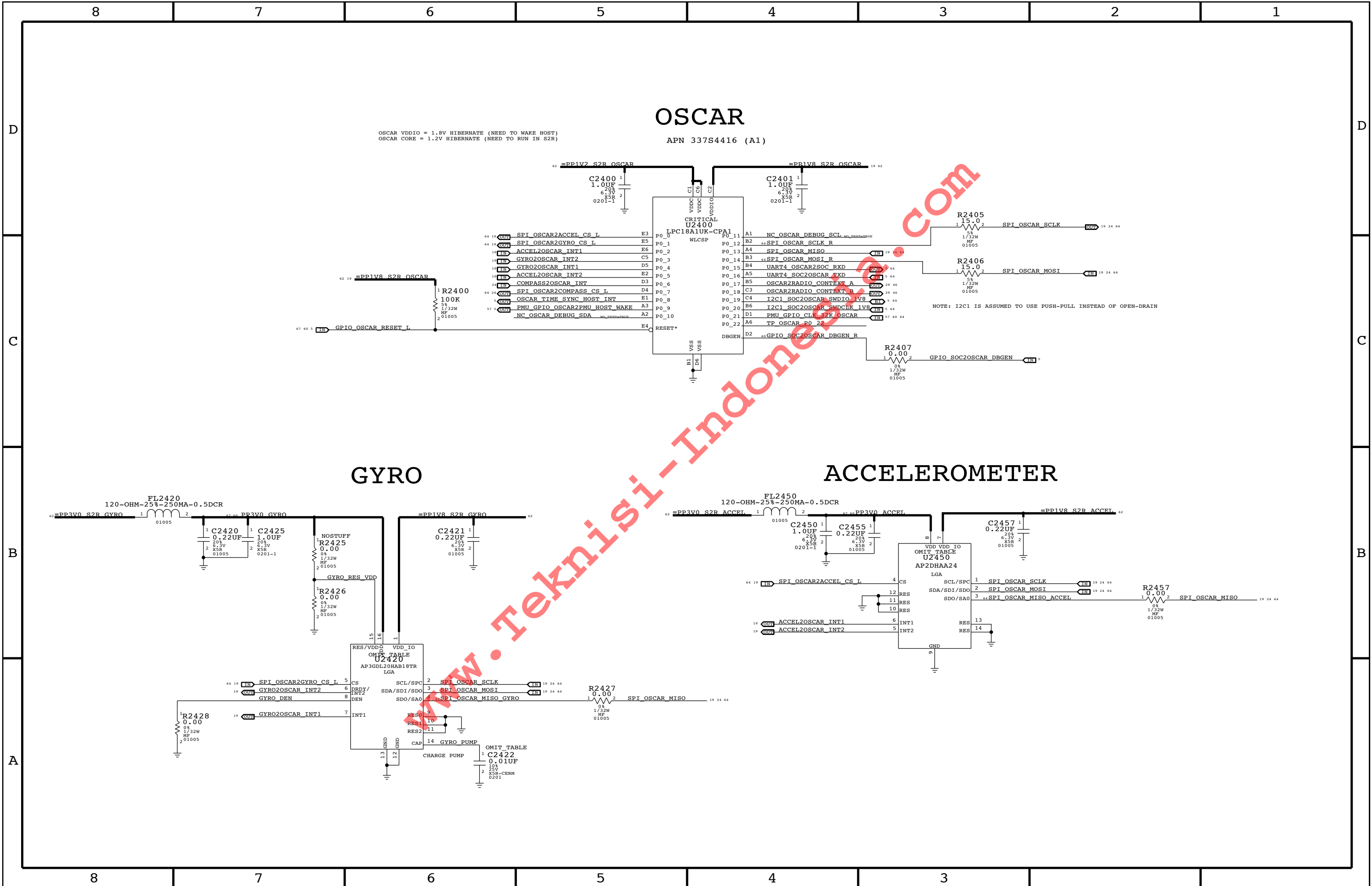
GAIN	VDD	GND
12DB	NC	SHORT
9DB	NC	100K
6DB	SHORT	NC
3DB	100K	NC
0DB	NC	NC

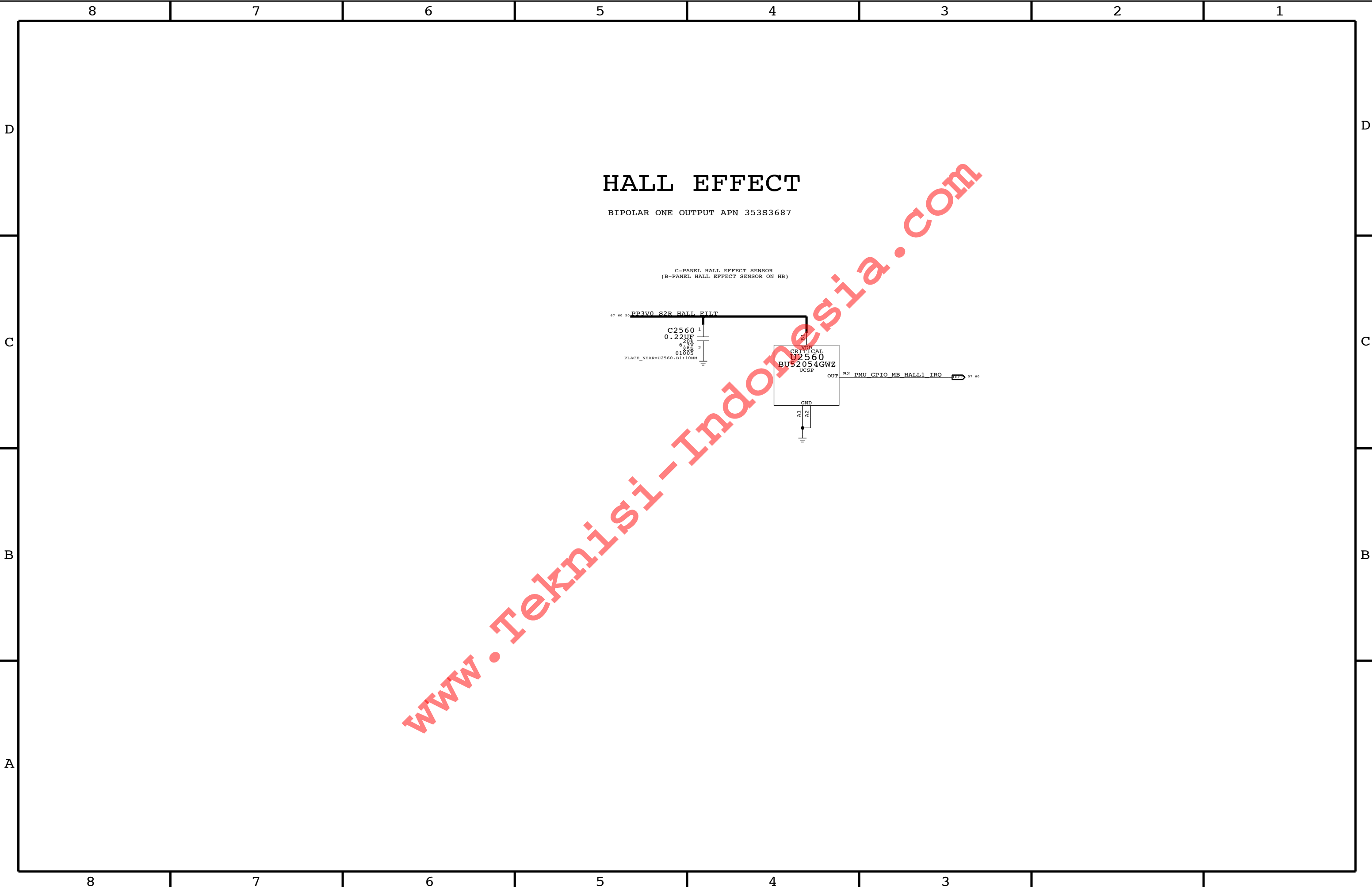
www.Teknisi.com

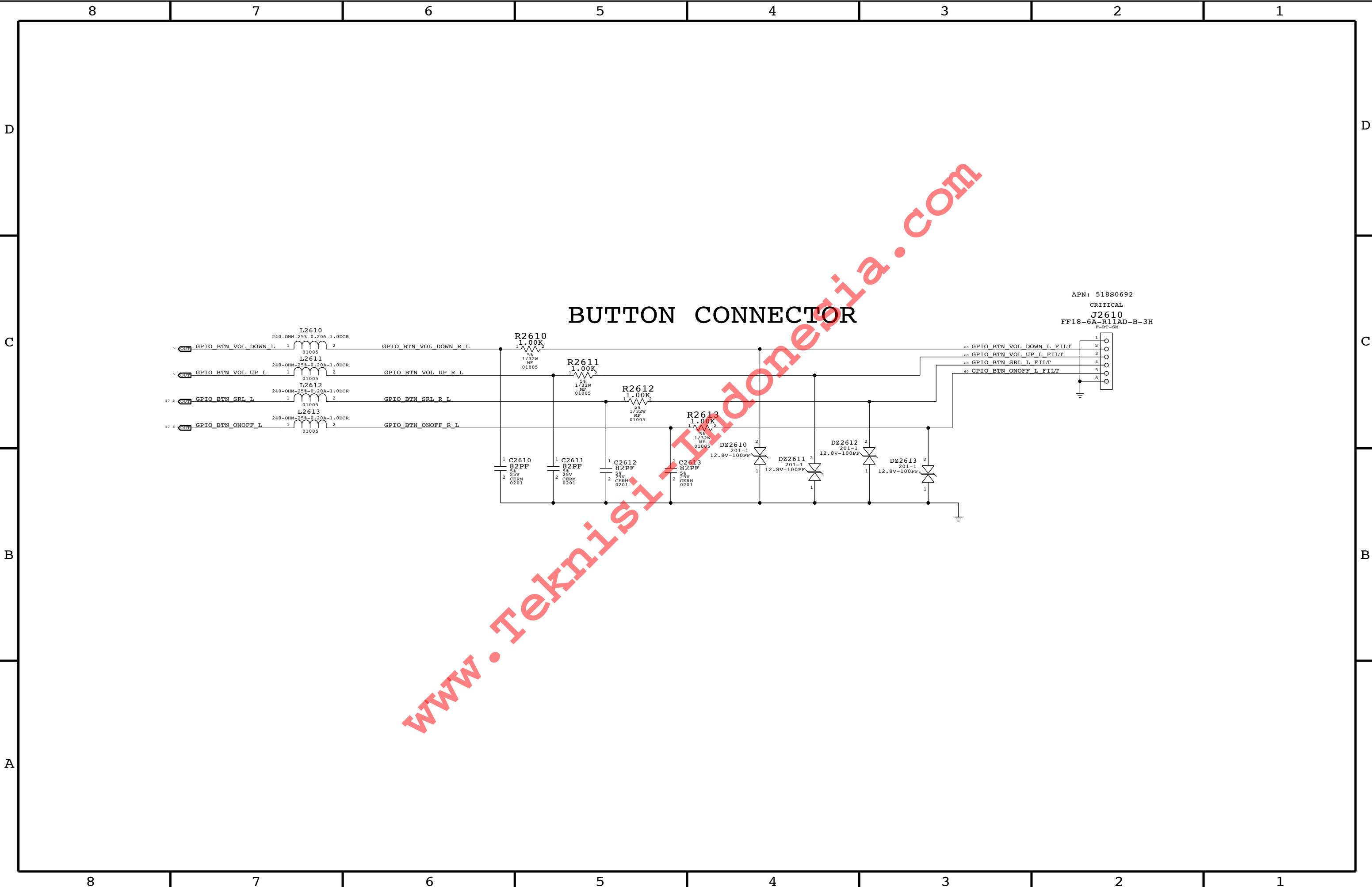
SPEAKER AMPLIFIER

APN: 353S3445
TURN ON TIME: 3.5MS
TURN ON DELAY: ?MS
75HZ +/- XXX%

GAIN	VDD	GND
12DB	NC	SHORT
9DB	NC	100K
6DB	SHORT	NC
3DB	100K	NC
0DB	NC	NC





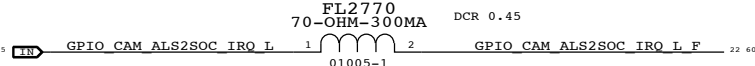
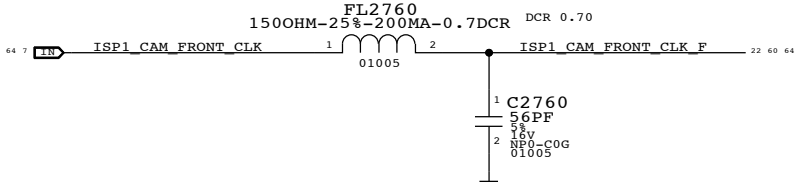
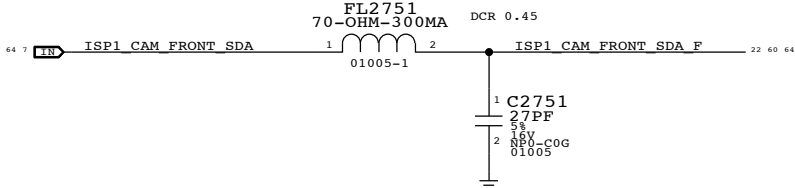
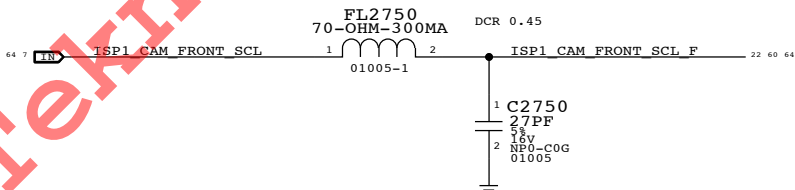
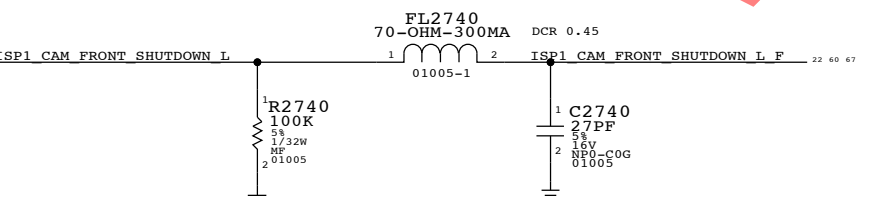
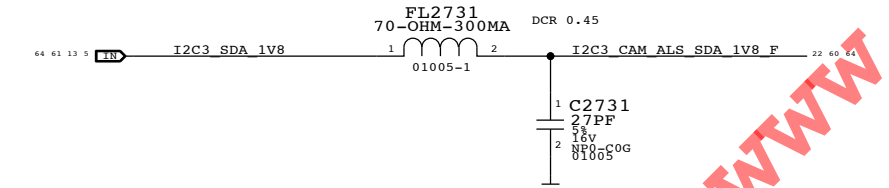
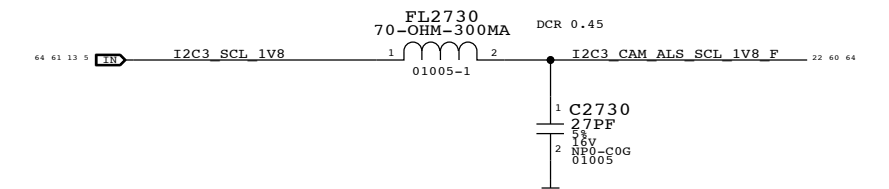
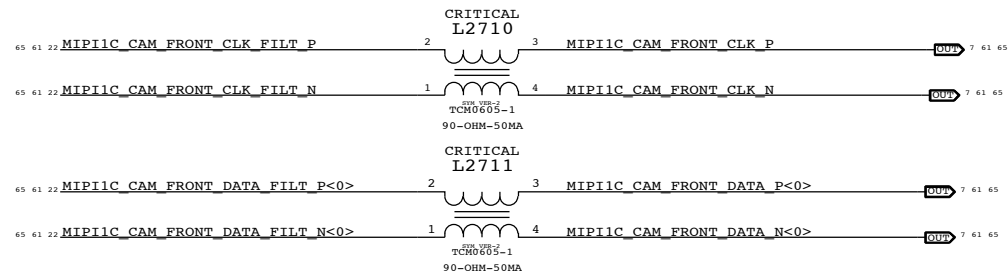
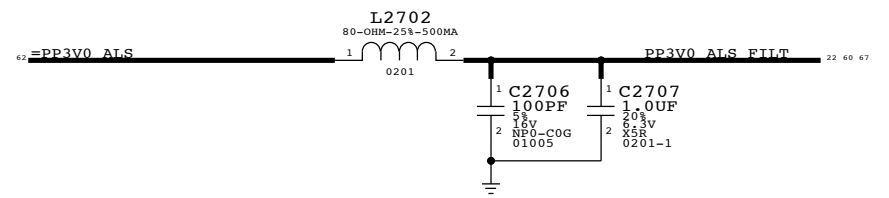
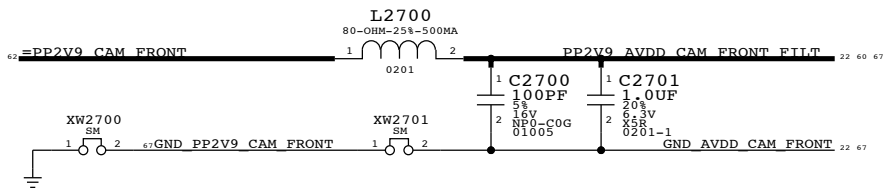
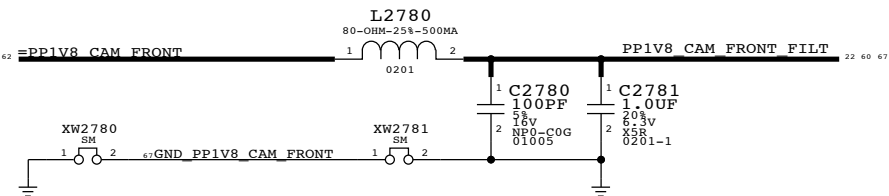
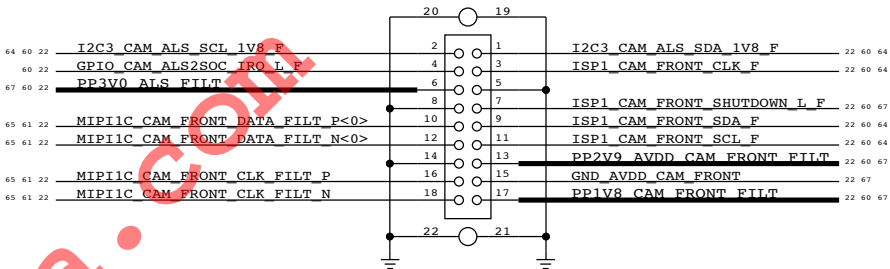


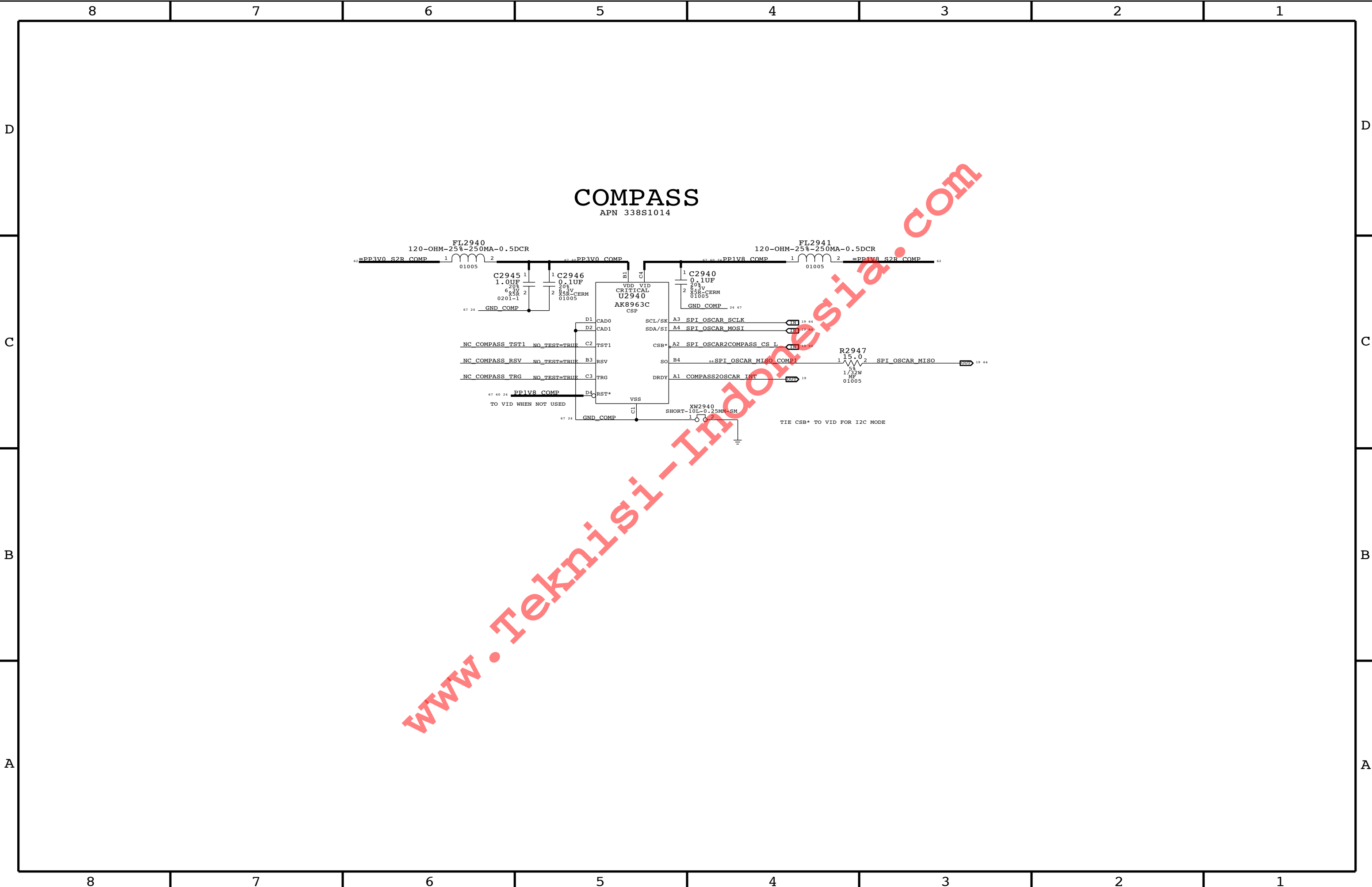
FRONT CAMERA CONNECTOR

J65 CAMERA CONNECTOR

APN:MLB 516S0876
APN:FLEX 516S0869

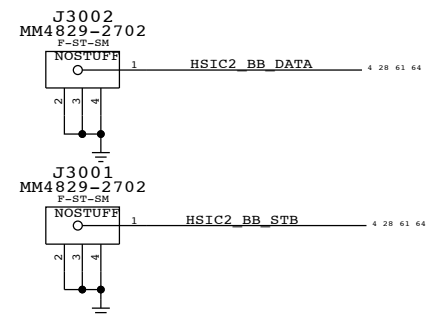
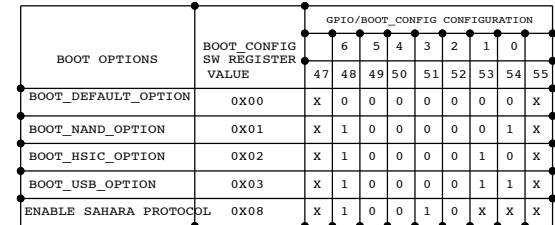
CRITICAL
J2700
503548-1820
F-ST-SH





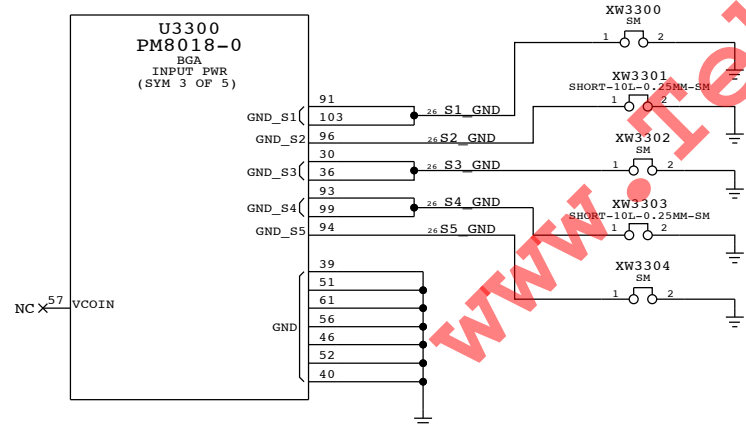
CONFIDENTIAL AND PROPRIETARY APPLE SYSTEM DESIGN. FOR REFERENCE PURPOSES ONLY - NOT A CHANGE REQUEST.

PP3000		
P4MM		
29	1 BB ERROR FLAG	29 68
PP3001		
P4MM		
29	1 SLEEP_CLK 32K	27 28 68
PP3002		
P4MM		
29	1 PMIC SSBI	27 28 68
PP3003		
P4MM		
29	1 19P2M MDM	27 28 68
PP3008		
P4MM		
29	1 WTR SSBI TX GPS	29 30
PP3009		
P4MM		
29	1 WTR SSBI PRX DRX	29 30
PP3010		
P4MM		
29	1 WTR RX ON	29 30 68
PP3011		
P4MM		
29	1 WTR RF ON	29 30 68
PP3012		
P4MM		
29	1 UART WLAN2BB LTE COEX	29 46
PP3013		
P4MM		
29	1 UART BB2WLAN LTE COEX	29 46

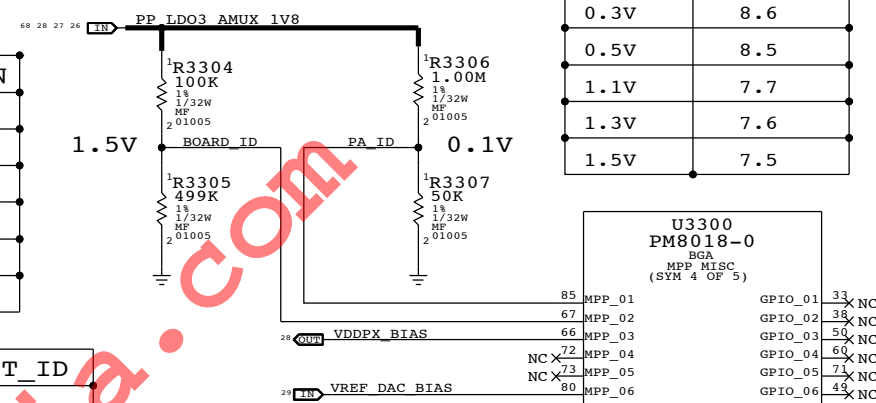


A

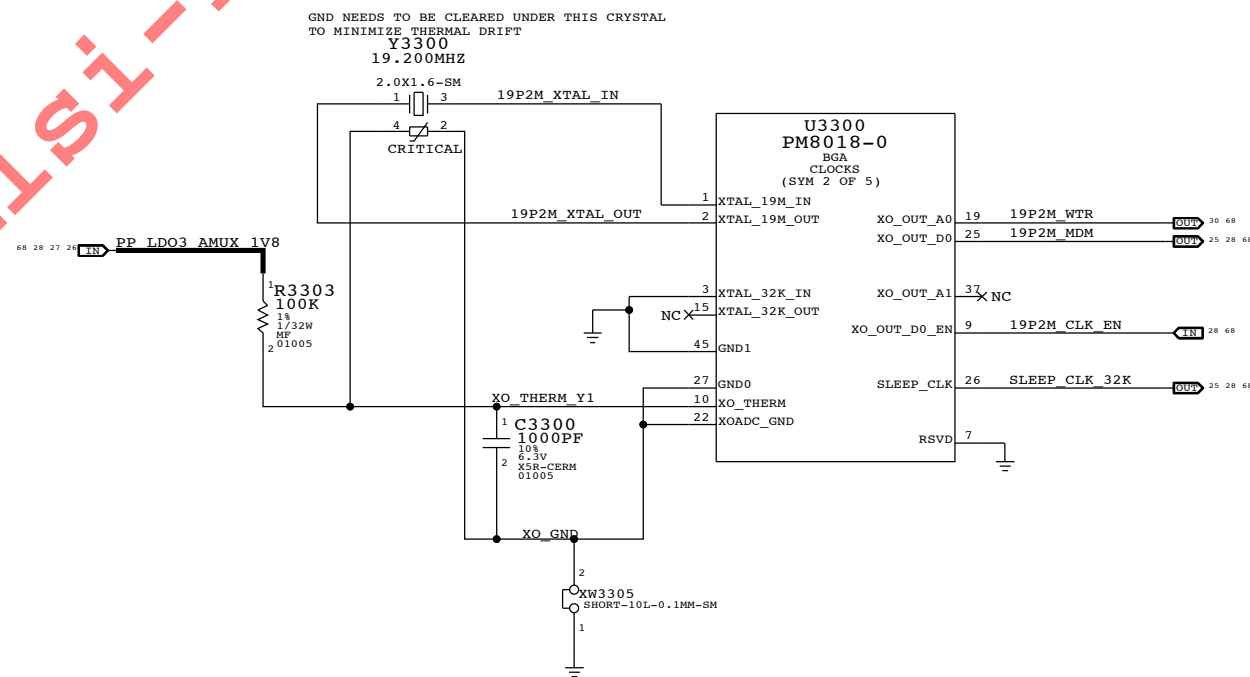
CONFIDENTIAL AND PROPRIETARY APPLE SYSTEM DESIGN. FOR REFERENCE PURPOSES ONLY - NOT A CHANGE REQUEST.



BB GPIO_29	PRODUCT_ID
1 (1.8V)	JXX
0 (NC, PD)	NXX



PA THERMISTOR REMOVED TO MATCH N41, AP SECTION
NEEDS ITS OWN THERMISTOR PLACED NEAR THE PA'S.



BASEBAND (1 OF 2)

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D

D

C

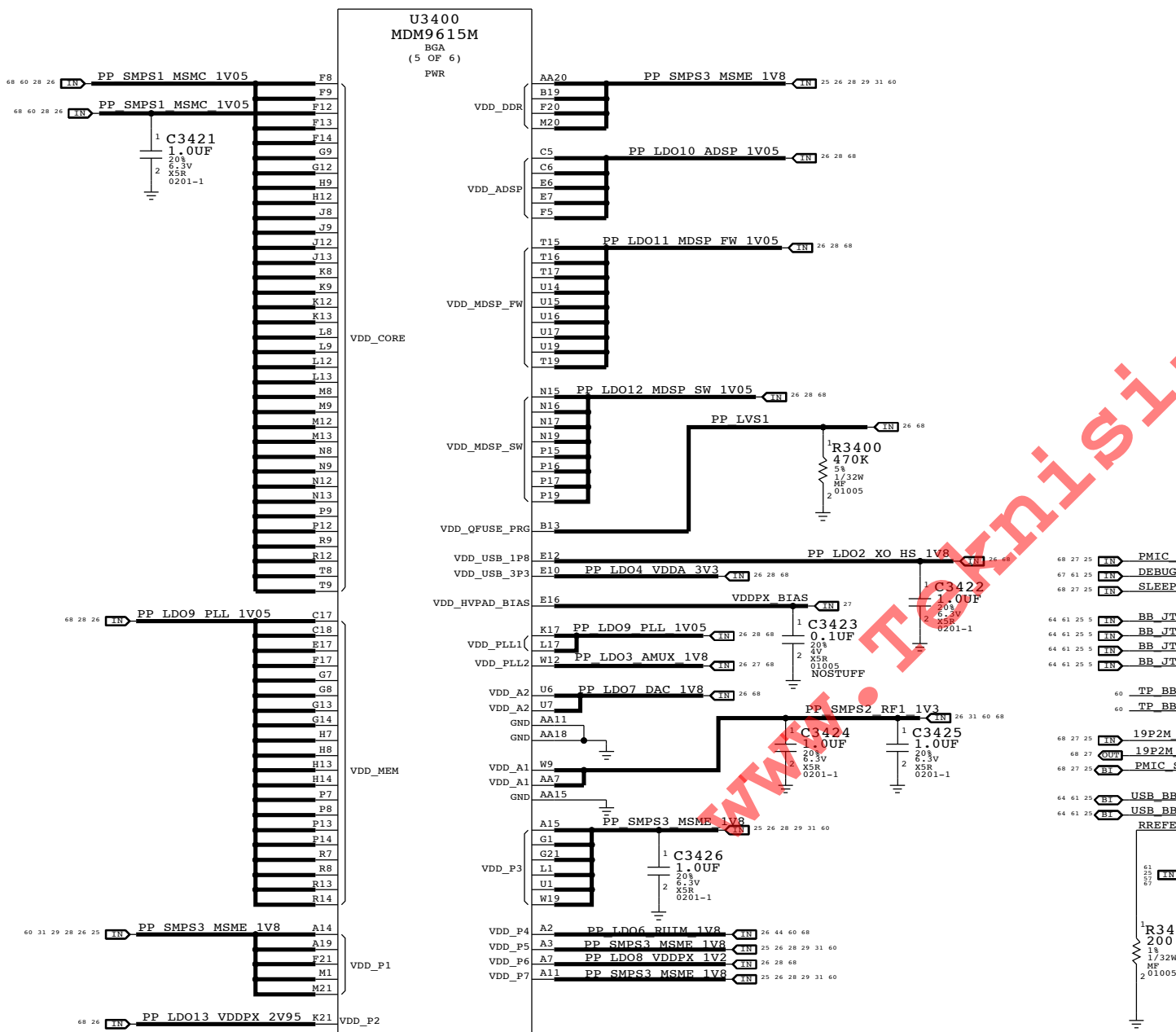
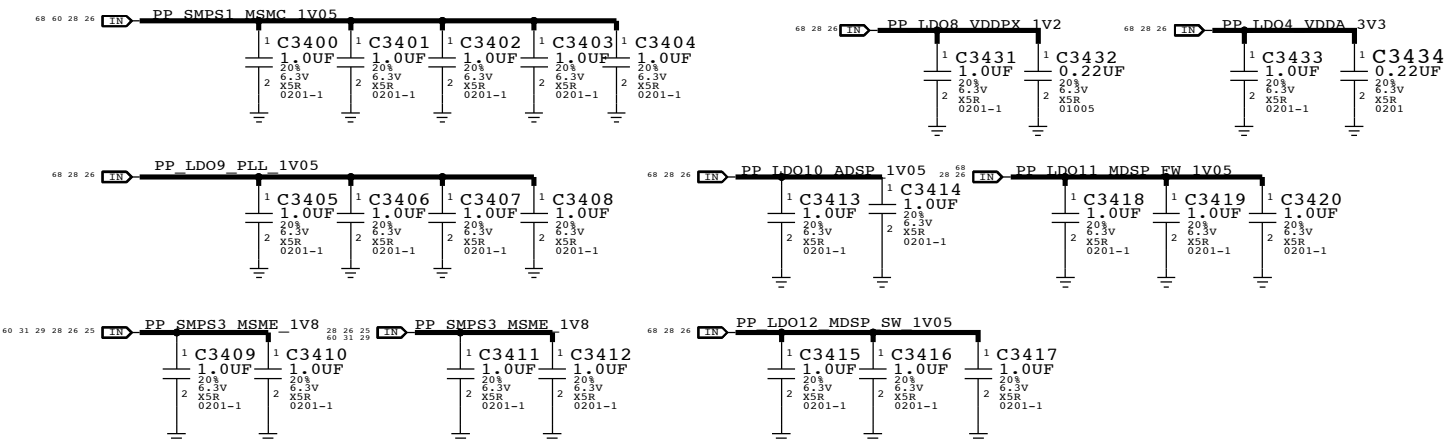
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B

B

A

A



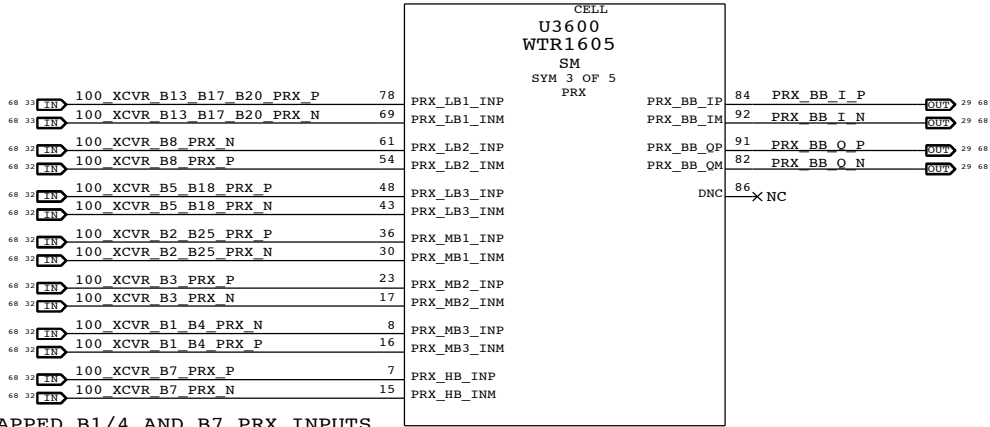
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CONFIDENTIAL AND PROPRIETARY APPLE SYSTEM DESIGN. FOR REFERENCE PURPOSES ONLY - NOT A CHANGE REQUEST.

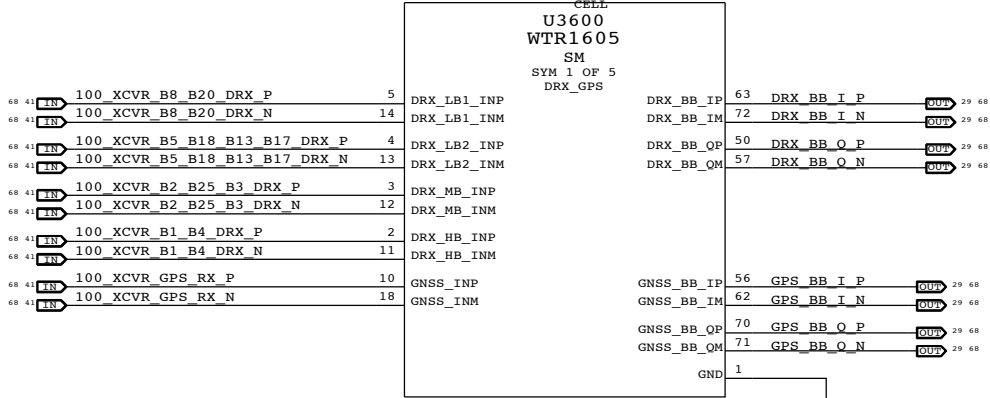
RF TRANSCEIVER (1 OF 2)

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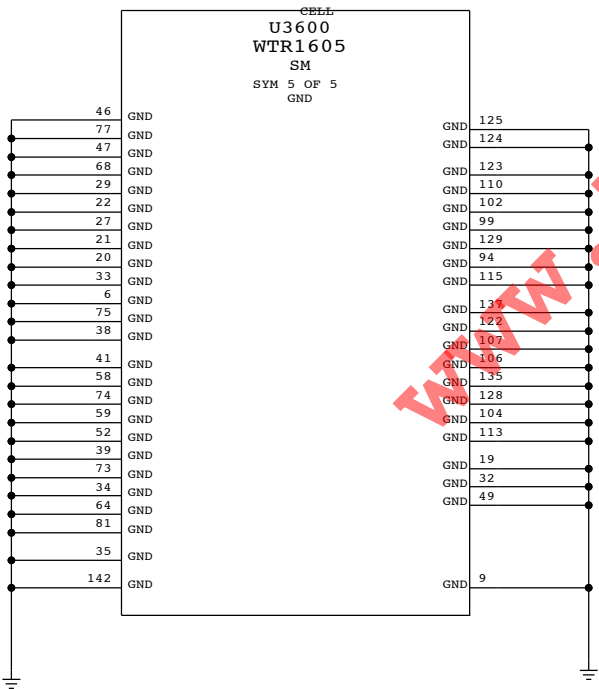
PRX TRANSCEIVER RF AND IQ PORTS



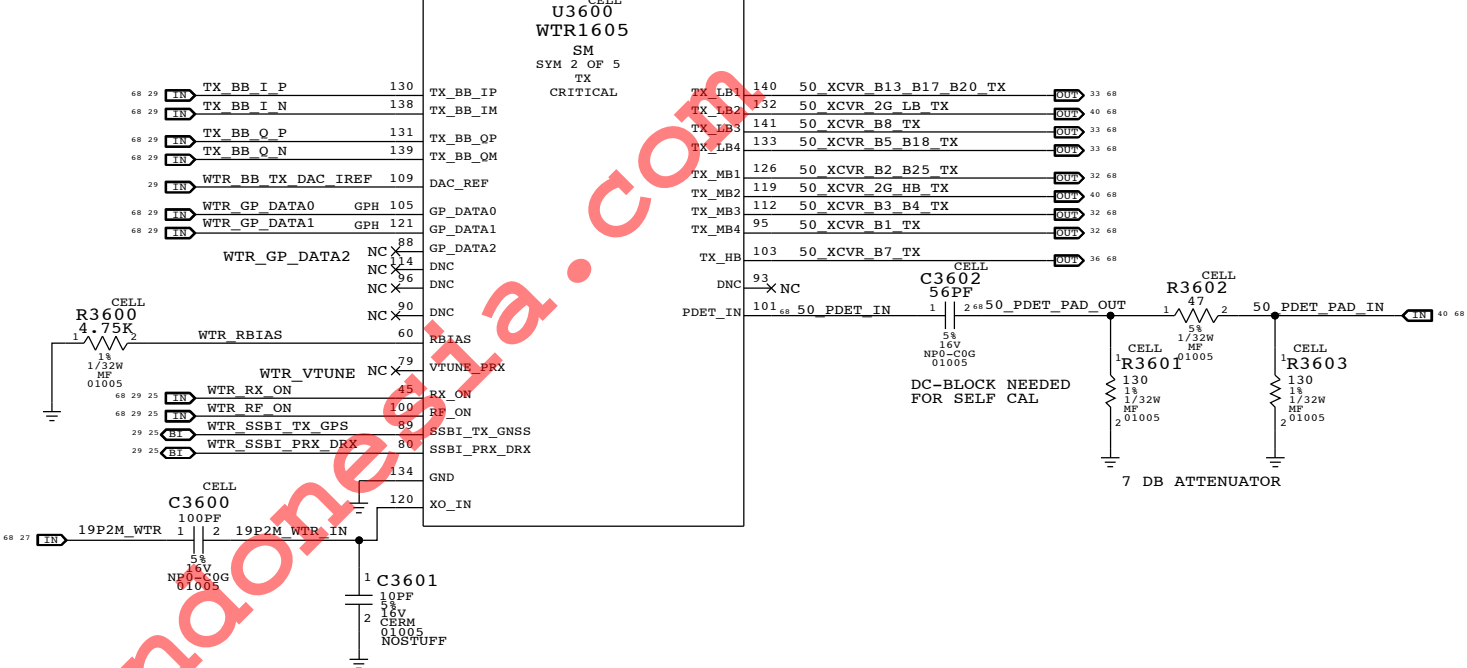
DRX TRANSCEIVER RF AND IQ PORTS



TRANSCEIVER GROUND CONNECTIONS

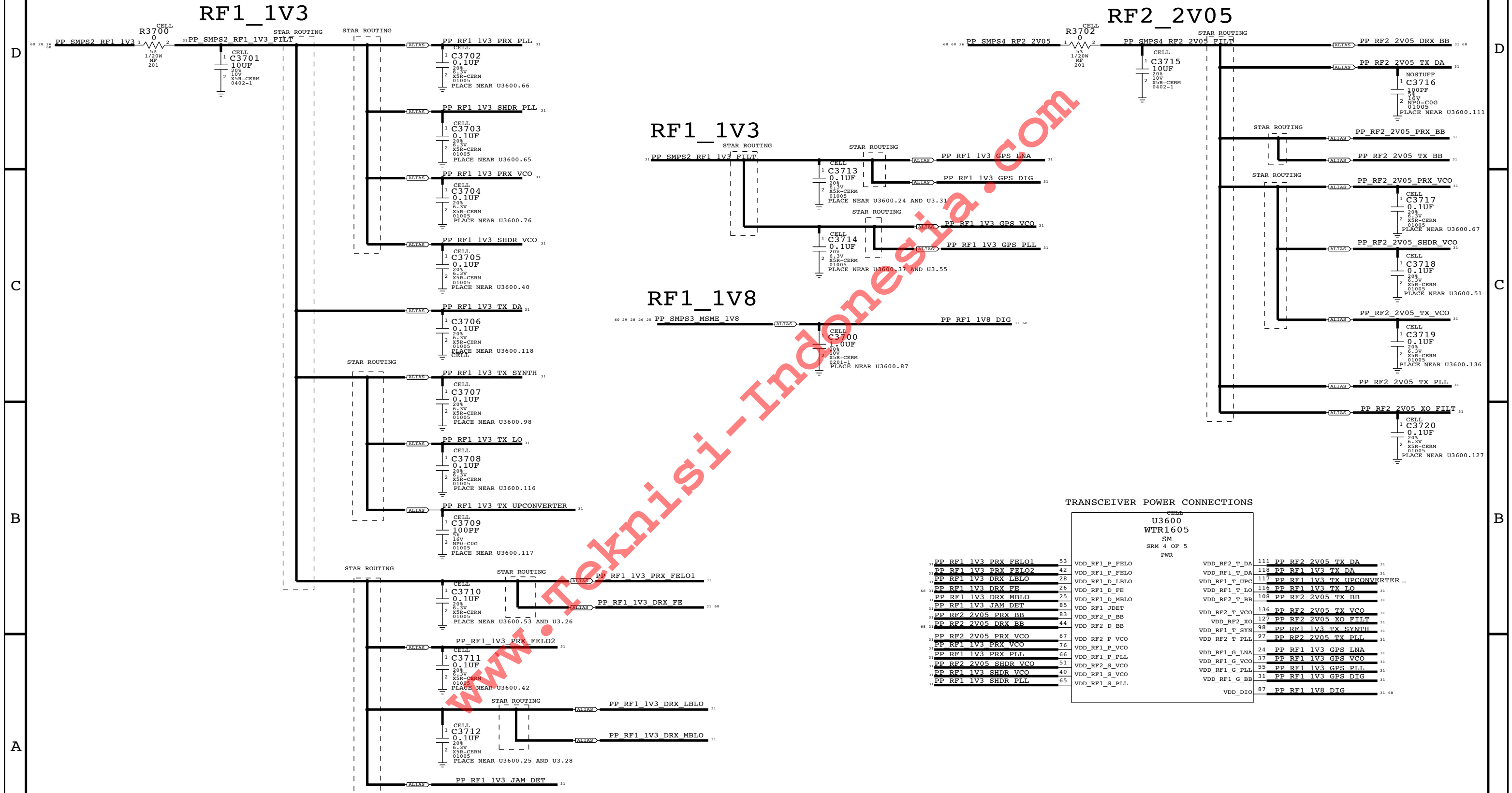


TRANSCEIVER PHASE CONTROL, TX RF & IQ PORTS



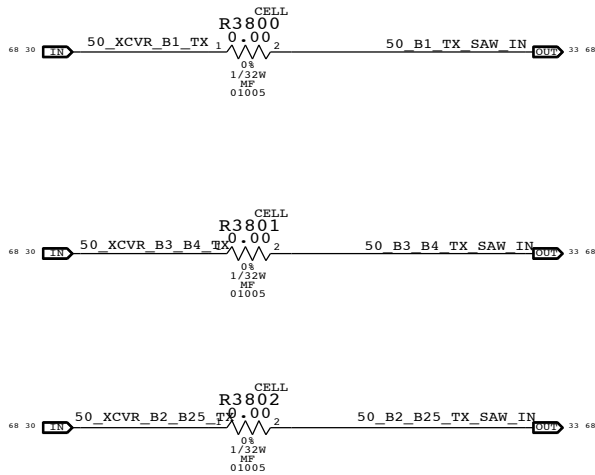
RF TRANSCEIVER (2 OF 2)

CONFIDENTIAL AND PROPRIETARY APPLE SYSTEM DESIGN. FOR REFERENCE PURPOSES ONLY - NOT A CHANGE REQUEST.

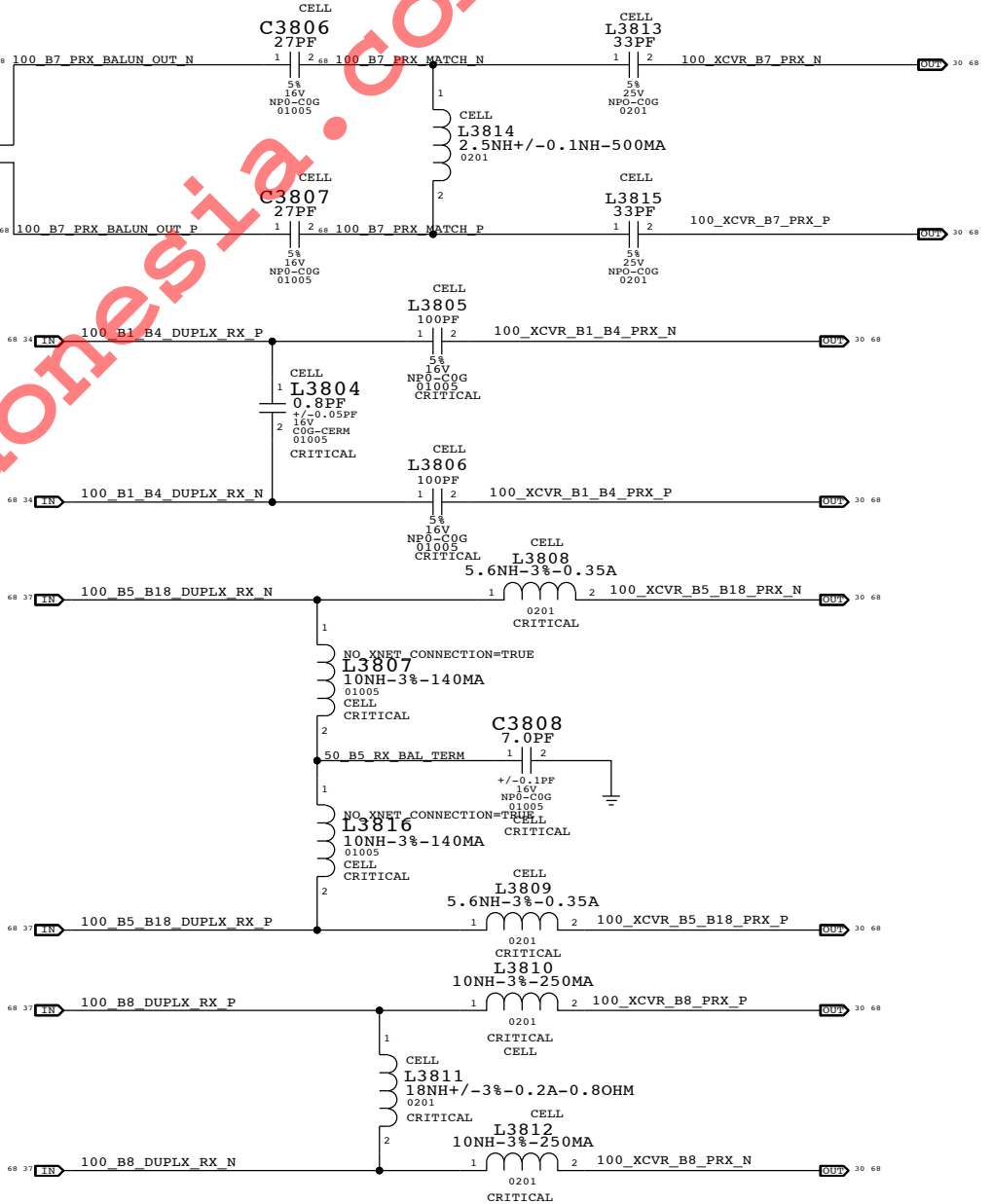
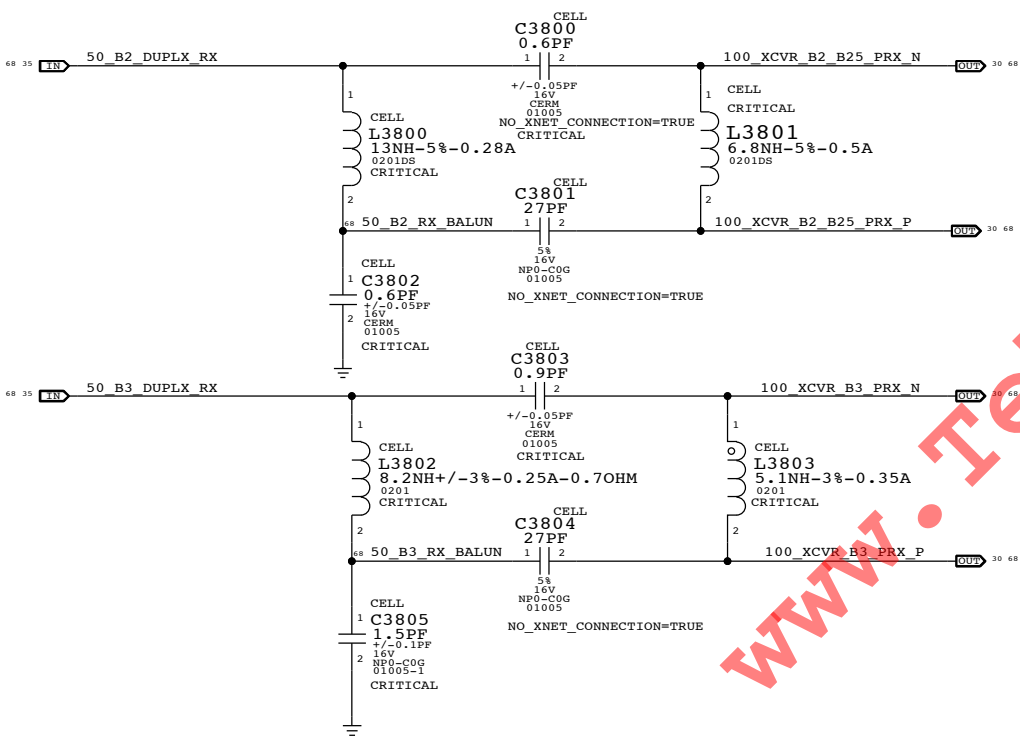


TRANSCEIVER TX AND RX MATCHING NETWORKS

TX MATCHING NETWORKS



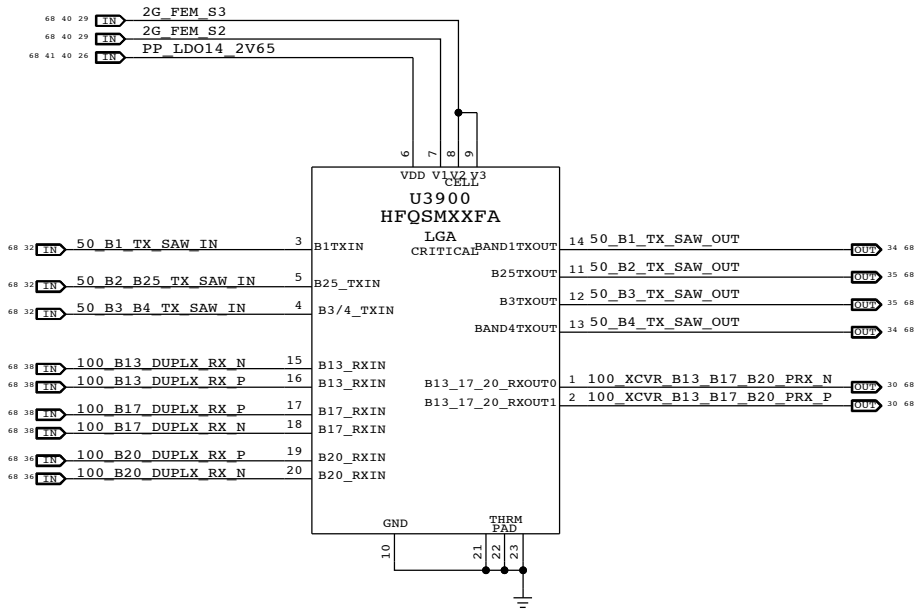
RX MATCHING NETWORKS



SAW BANK

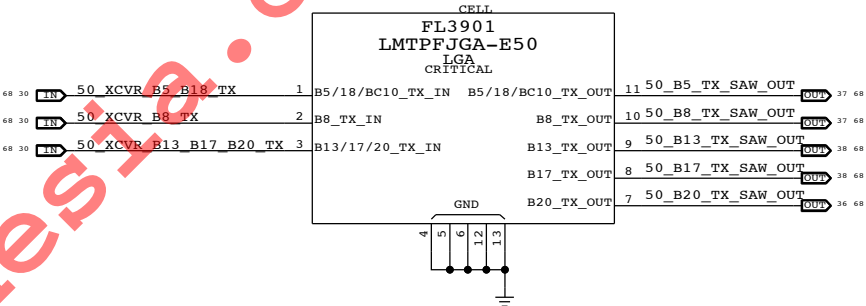
CONFIDENTIAL AND PROPRIETARY APPLE SYSTEM DESIGN. FOR REFERENCE PURPOSES ONLY - NOT A CHANGE REQUEST.

HB TX SAW BANK + B13/B17/B20 DP6T SWITCH AND MATCHING



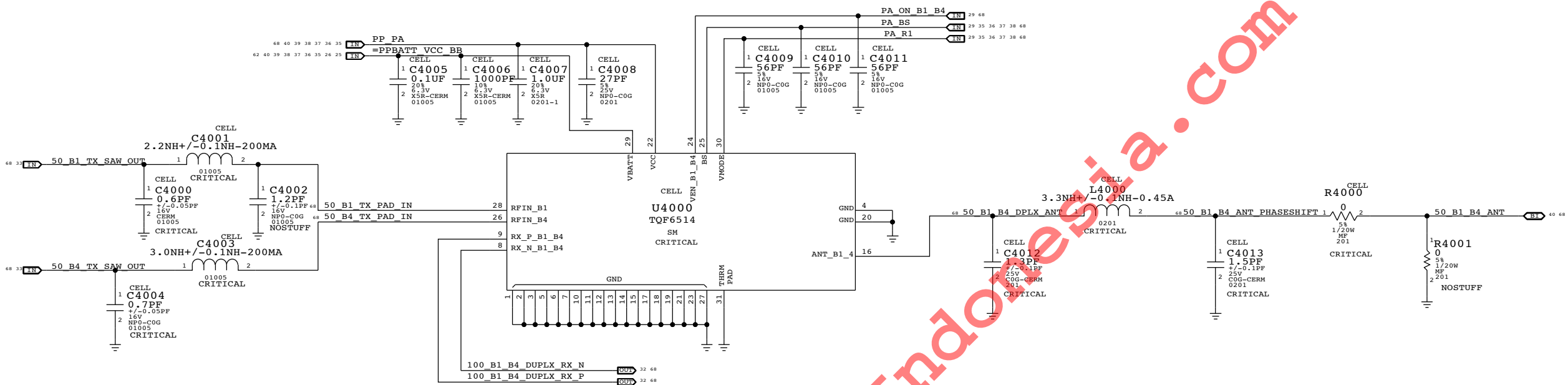
BAND	V3=V2	V1
B3 TX	HIGH	X
B4 TX	LOW	X
B13 RX	HIGH	HIGH
B17 RX	HIGH	LOW
B20 RX	LOW	HIGH

LB TX SAW BANK



BAND 1/4 PAD

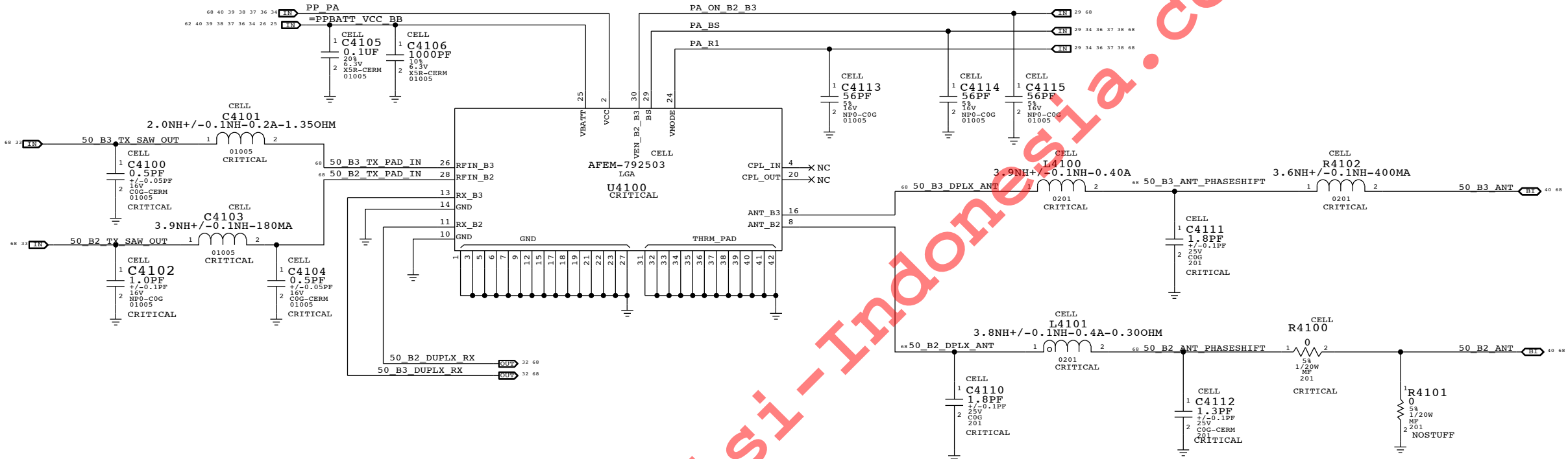
CONFIDENTIAL AND PROPRIETARY APPLE SYSTEM DESIGN. FOR REFERENCE PURPOSES ONLY - NOT A CHANGE REQUEST.



BAND	PA POWER MODE	PA BS	PA_ON	B1	B4	PA_R1
=====	=====	=====	=====	=====	=====	=====
POWER DOWN	X	0	0			0
STANDBY	X	X	0			X
B4	HPM	0	1			0
B4	LPM	0	1			1
B1	HPM	1	1			0
B1	LPM	1	1			1

BAND 2/3 PAD

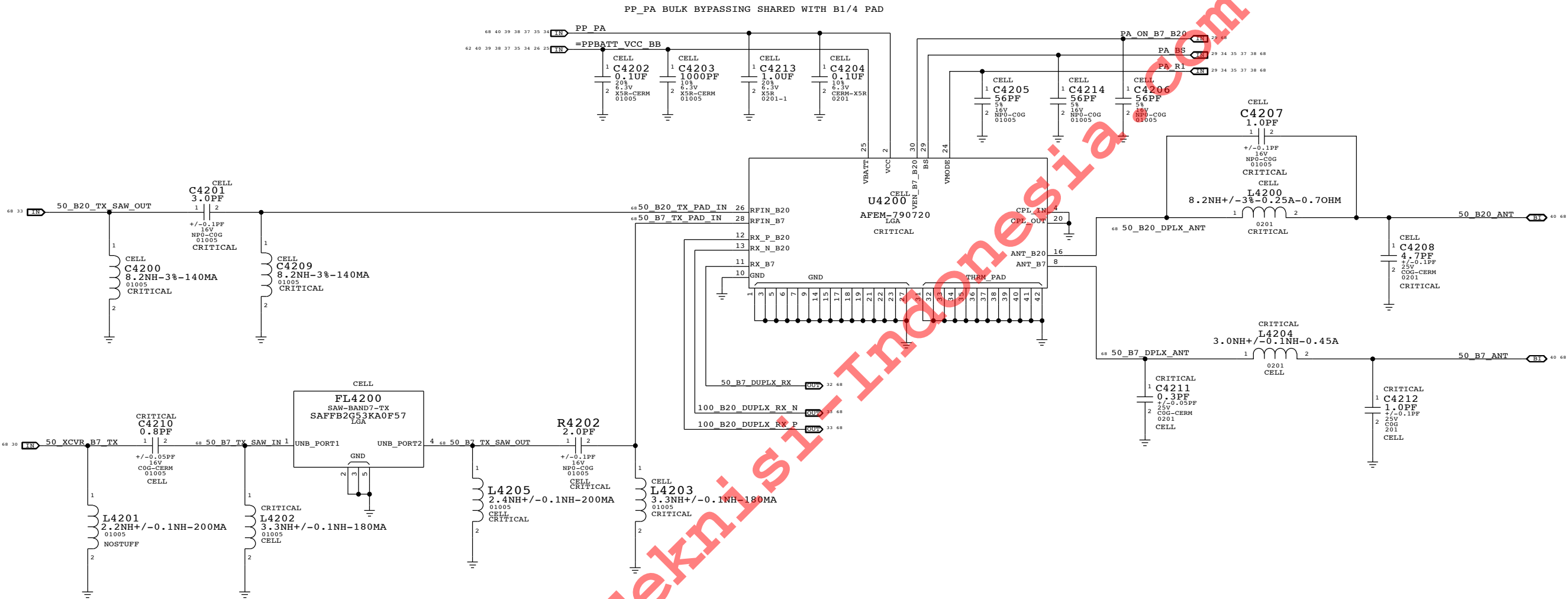
CONFIDENTIAL AND PROPRIETARY APPLE SYSTEM DESIGN. FOR REFERENCE PURPOSES ONLY - NOT A CHANGE REQUEST.



BAND	PA POWER MODE	PA BS	PA ON B2 B3	PA R1
=====	=====	=====	=====	=====
POWER DOWN	X	0	0	0
STANDBY	X	X	0	X
B3	HPM	0	1	0
B3	LPM	0	1	1
B2	HPM	1	1	0
B2	LPM	1	1	1

BAND 20/7 PAD

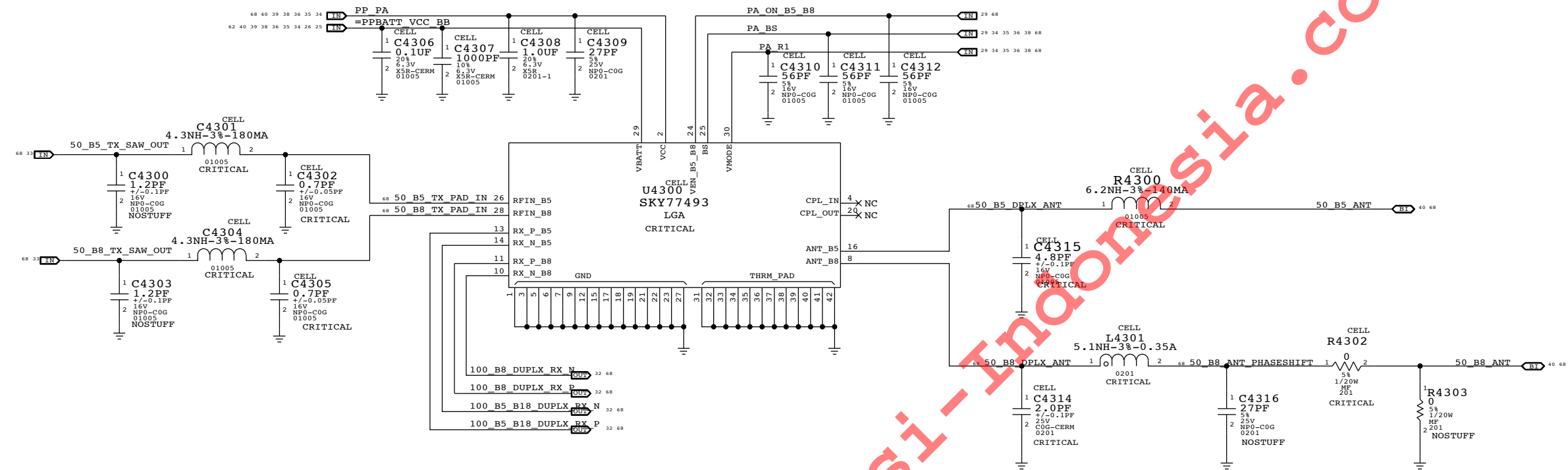
CONFIDENTIAL AND PROPRIETARY APPLE SYSTEM DESIGN. FOR REFERENCE PURPOSES ONLY - NOT A CHANGE REQUEST.



BAND	PA POWER MODE	PA ON B20	PA R1
=====	=====	=====	=====
POWER DOWN	LPM	0	0
STANDBY	X	0	X
B20	HPM	1	0
B20	LPM	1	1

BAND 5/8 PAD

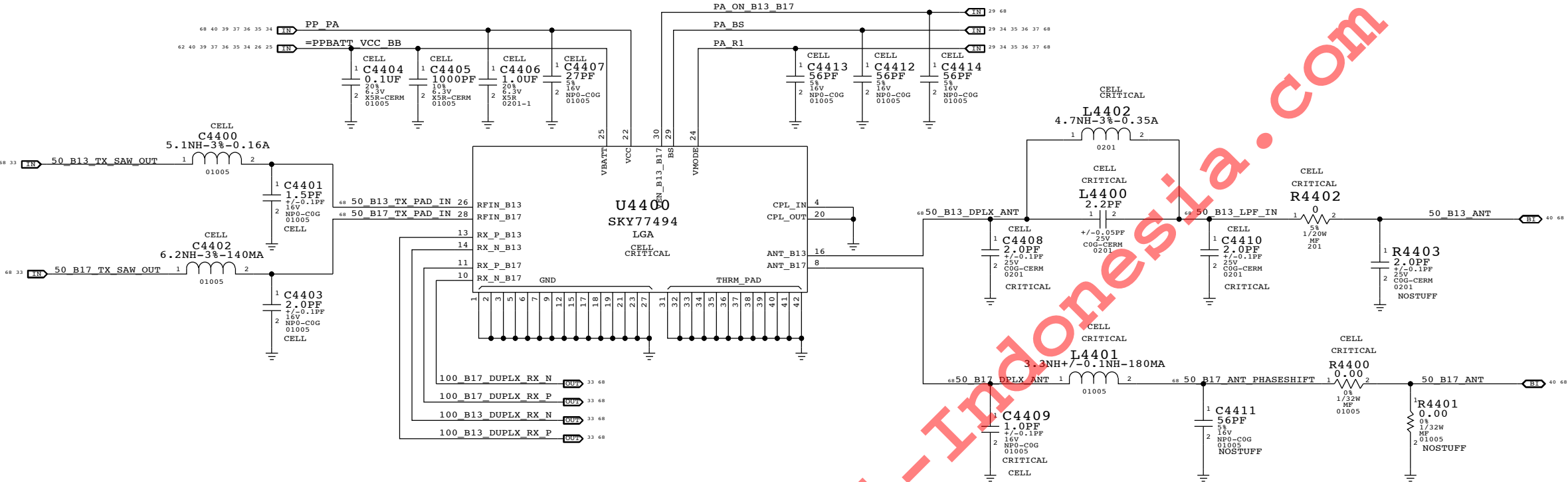
CONFIDENTIAL AND PROPRIETARY APPLE SYSTEM DESIGN. FOR REFERENCE PURPOSES ONLY - NOT A CHANGE REQUEST.



BAND	PA	POWER	MODE	PA	BS	PA	ON	B5	B8	PA	R1
=====	=====	=====	=====	=====	=====	=====	=====	=====	=====	=====	=====
POWER DOWN		X		0		0		0		0	
STANDBY		X		X		0		X			
B5		HPM		0		1		0			
B5		LPM		0		1		1			
B8		HPM		1		1		0			
B8		LPM		1		1		1			

BAND 13/17 PAD

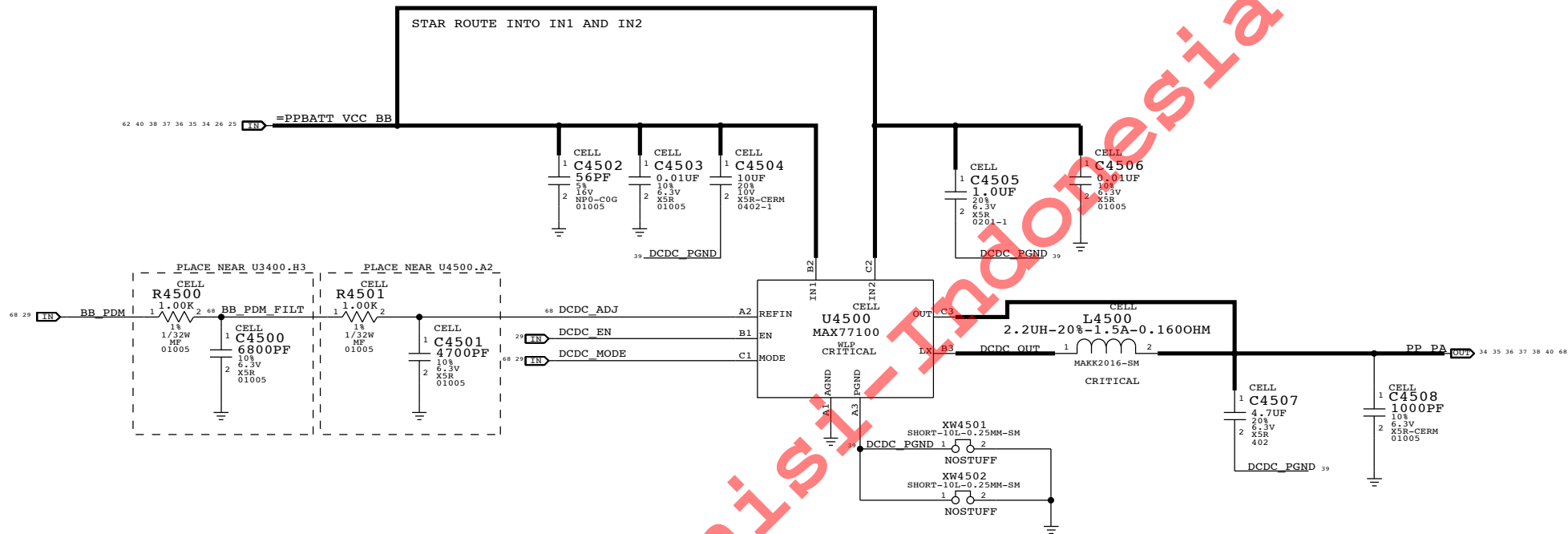
CONFIDENTIAL AND PROPRIETARY APPLE SYSTEM DESIGN. FOR REFERENCE PURPOSES ONLY - NOT A CHANGE REQUEST.



BAND	PA POWER MODE	PA BS	PA ON B13 B17	PA R1
=====	=====	=====	=====	=====
POWER DOWN	X	0	0	0
STANDBY	X	X	0	X
B17	HPM	0	1	0
B17	LPM	0	1	1
B13	HPM	1	1	0
B13	LPM	1	1	1

PA DC/DC CONVERTER

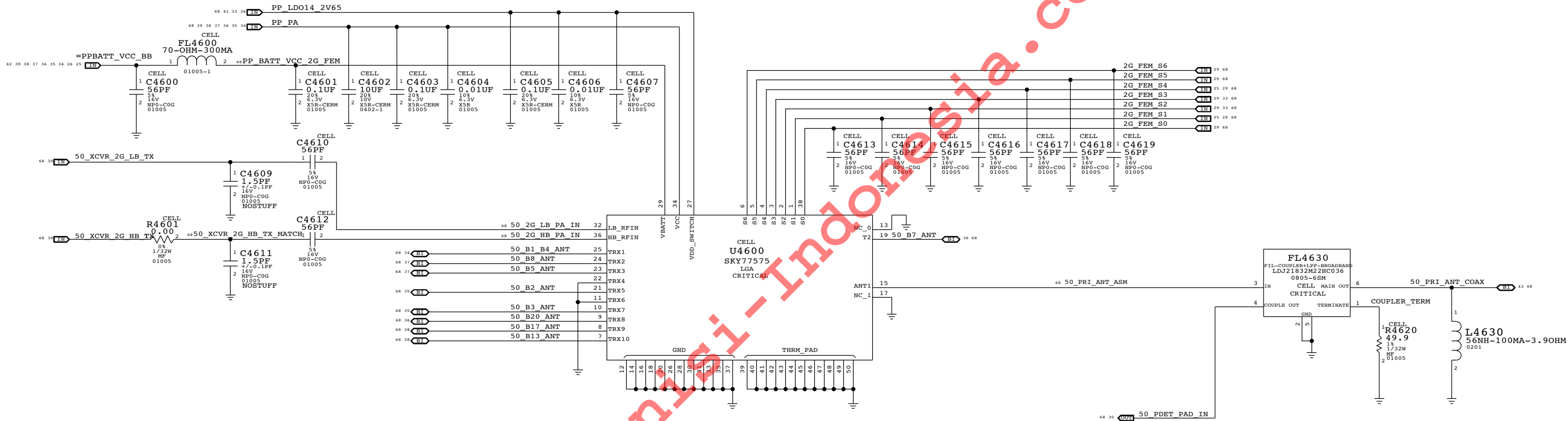
CONFIDENTIAL AND PROPRIETARY APPLE SYSTEM DESIGN. FOR REFERENCE PURPOSES ONLY - NOT A CHANGE REQUEST.



2G FEM

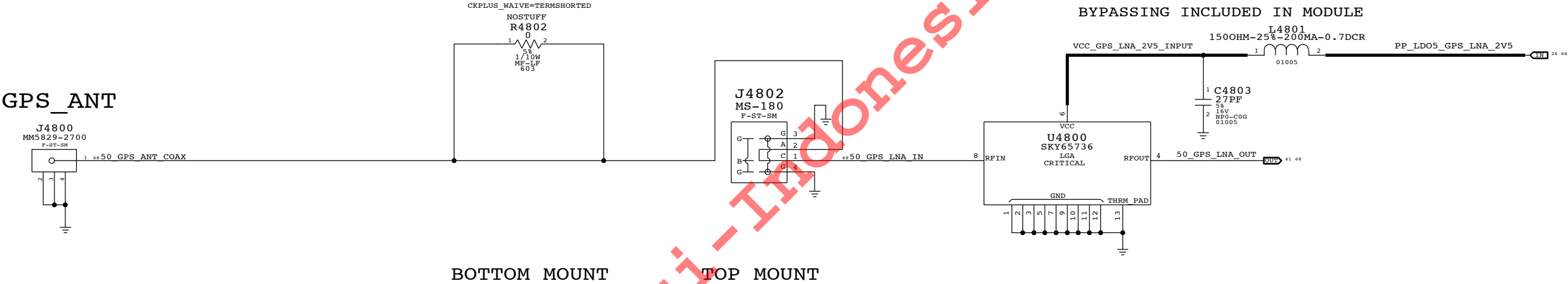
CONFIDENTIAL AND PROPRIETARY APPLE SYSTEM DESIGN. FOR REFERENCE PURPOSES ONLY - NOT A CHANGE REQUEST.

2G FEM



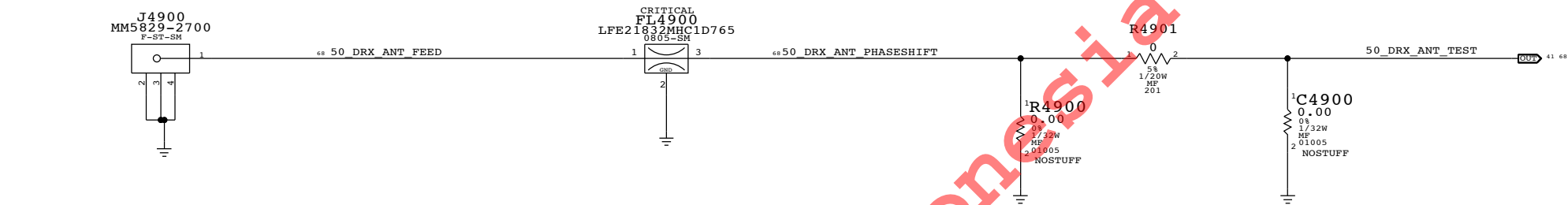
BAND	DRX_ASM_V4	DRX_ASM_V3	DRX_ASM_V2	DRX_ASM_V1
B1/B4	LOW	LOW	LOW	LOW
B2/25	LOW	HIGH	LOW	LOW
B3	HIGH	LOW	LOW	LOW
B5/6/18	LOW	LOW	HIGH	LOW
B8	LOW	LOW	LOW	HIGH
B13/17	LOW	HIGH	HIGH	HIGH
B20	LOW	HIGH	HIGH	LOW
OFF	LOW	LOW	HIGH	HIGH
SWITCH IS TERMINATED IN ALL OTHER POSSIBLE STATES				

GPS

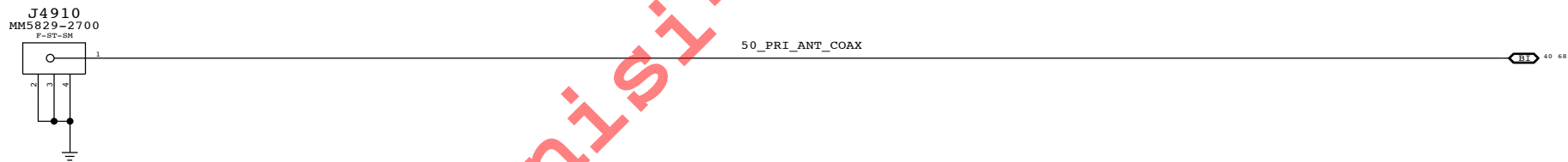


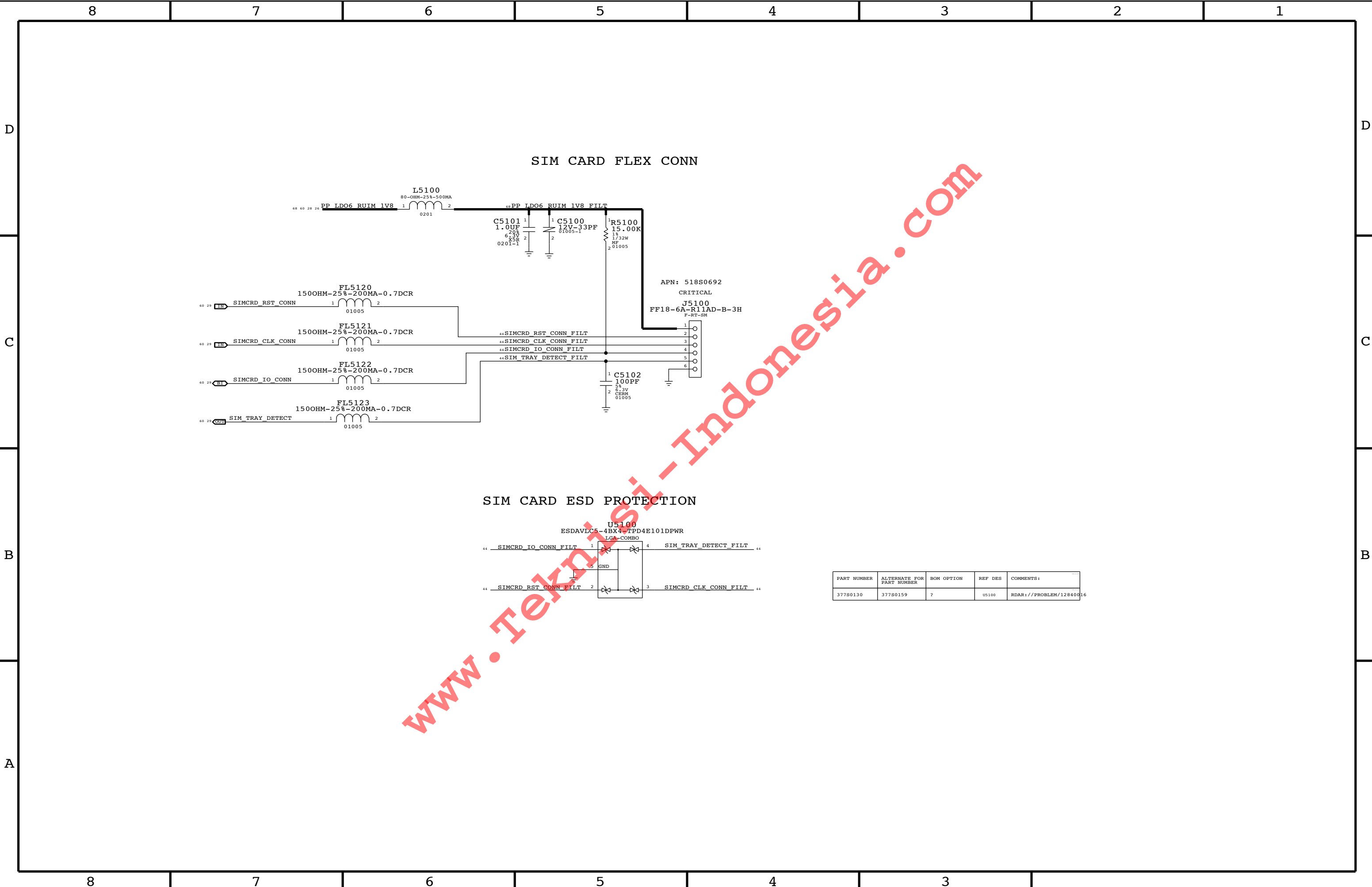
ANTENNA FEEDS

DRX_ANT COAX

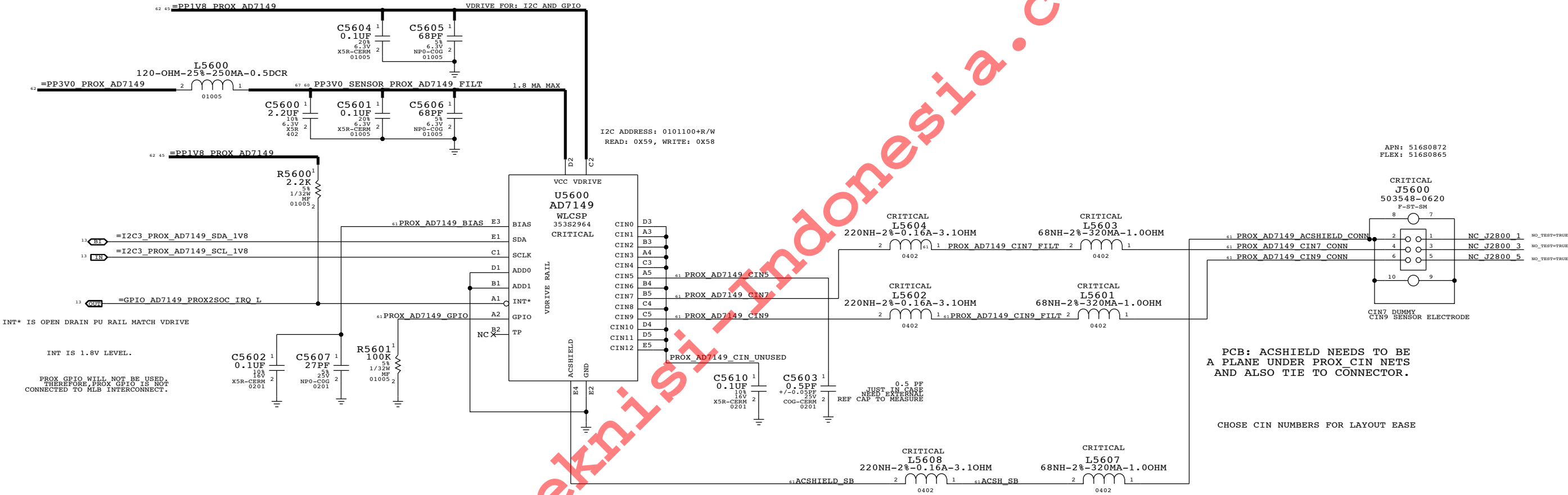


PRI_ANT COAX





PROX SENSOR

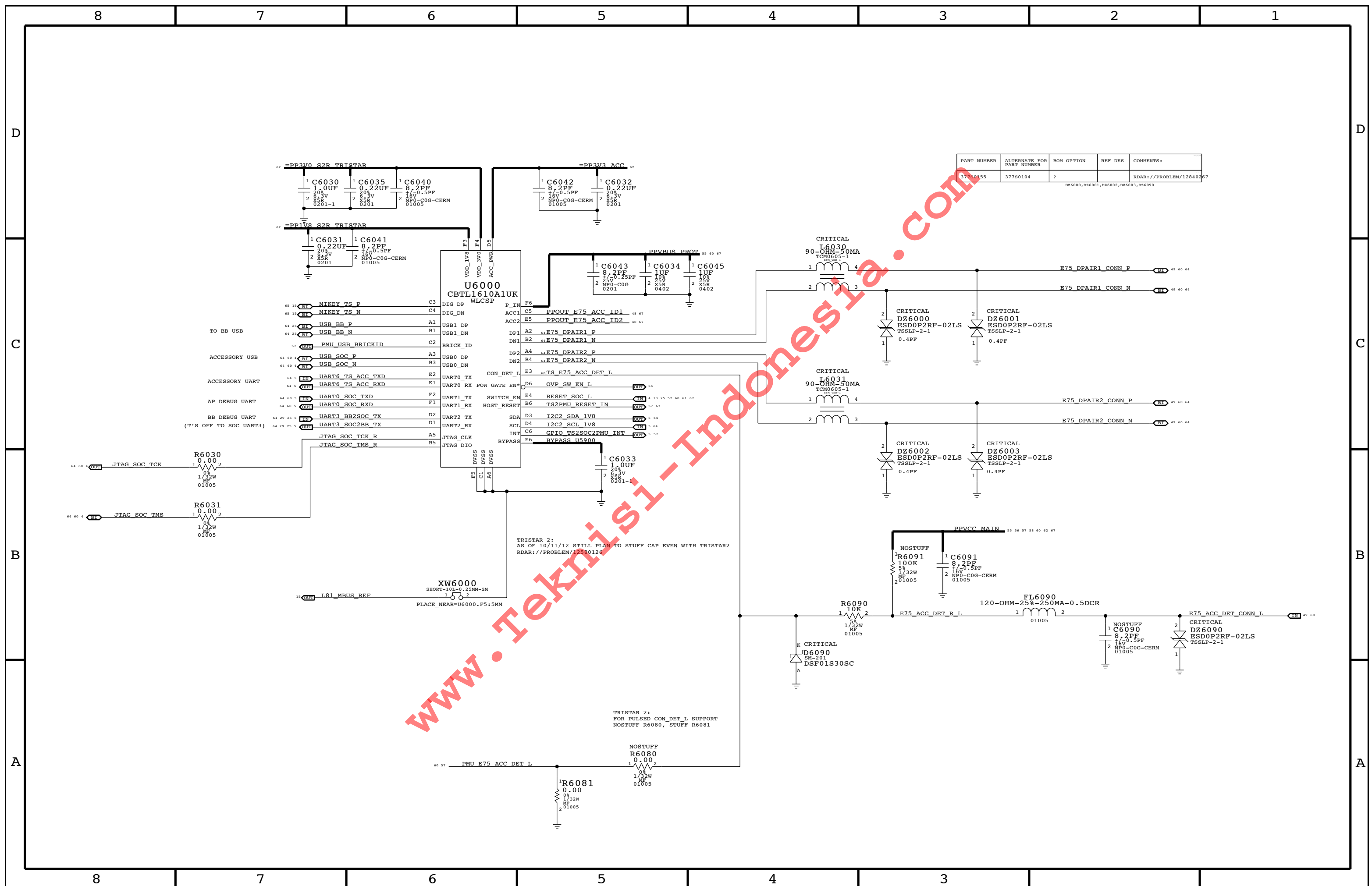


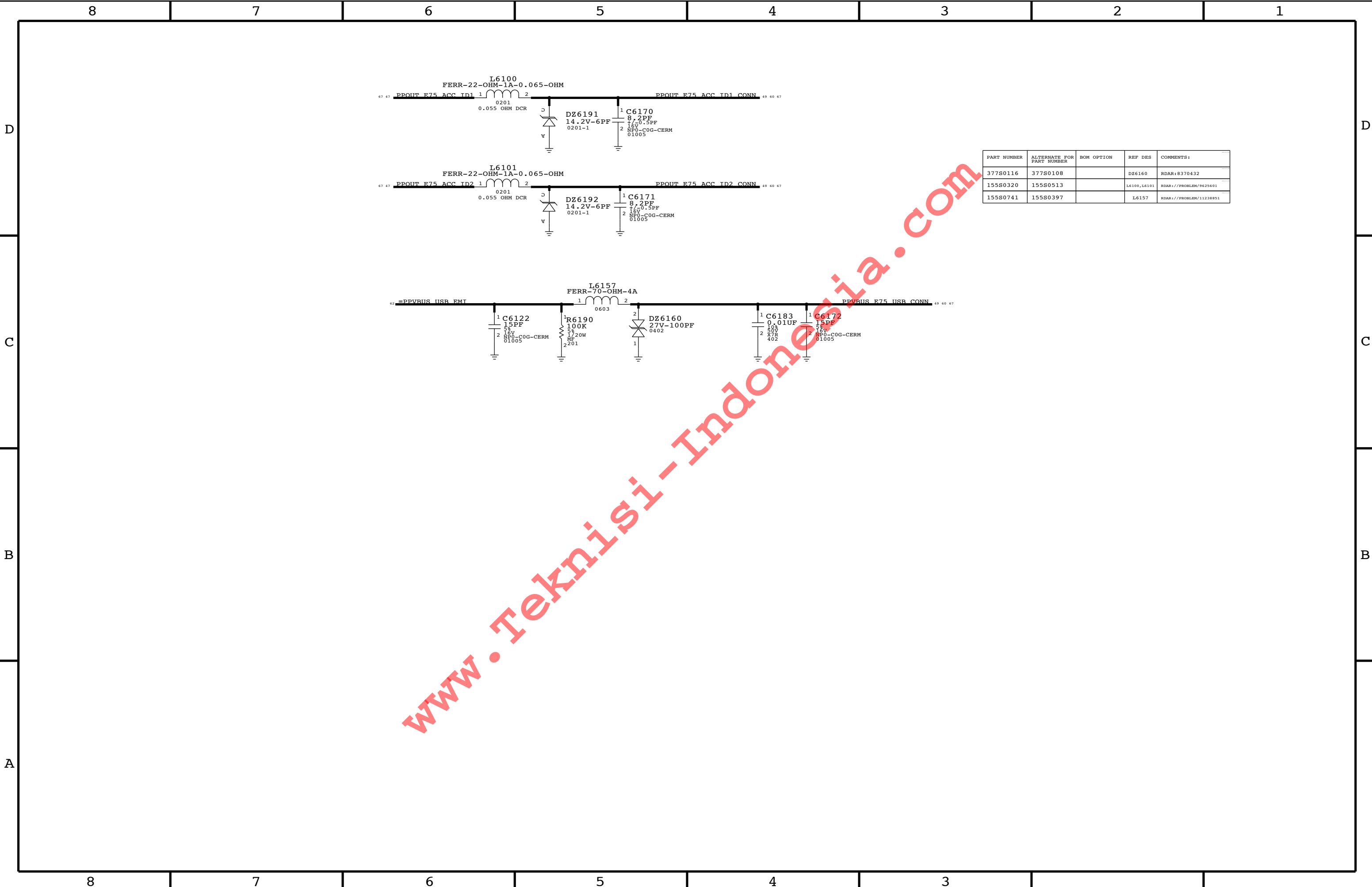
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D

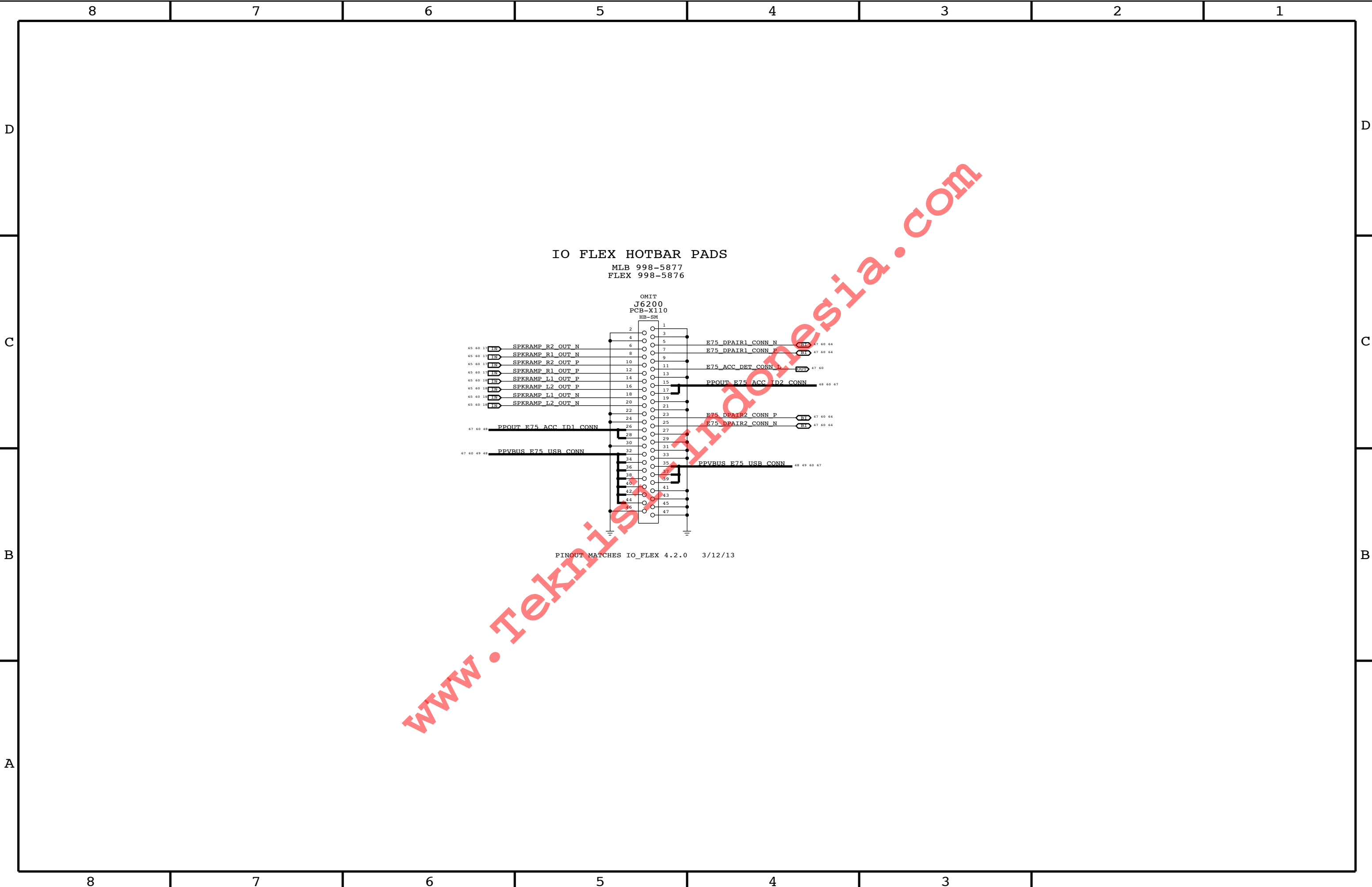


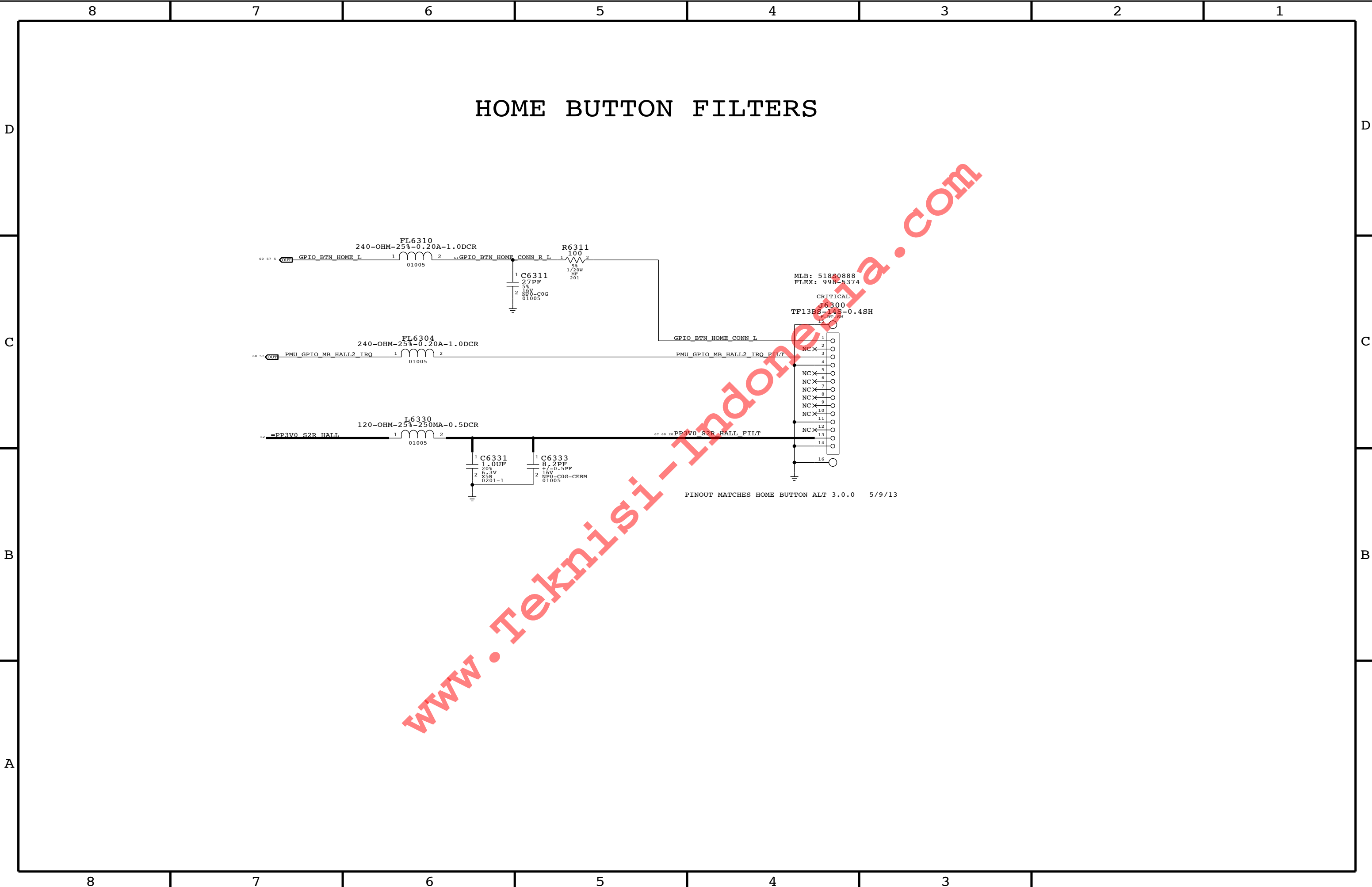
B

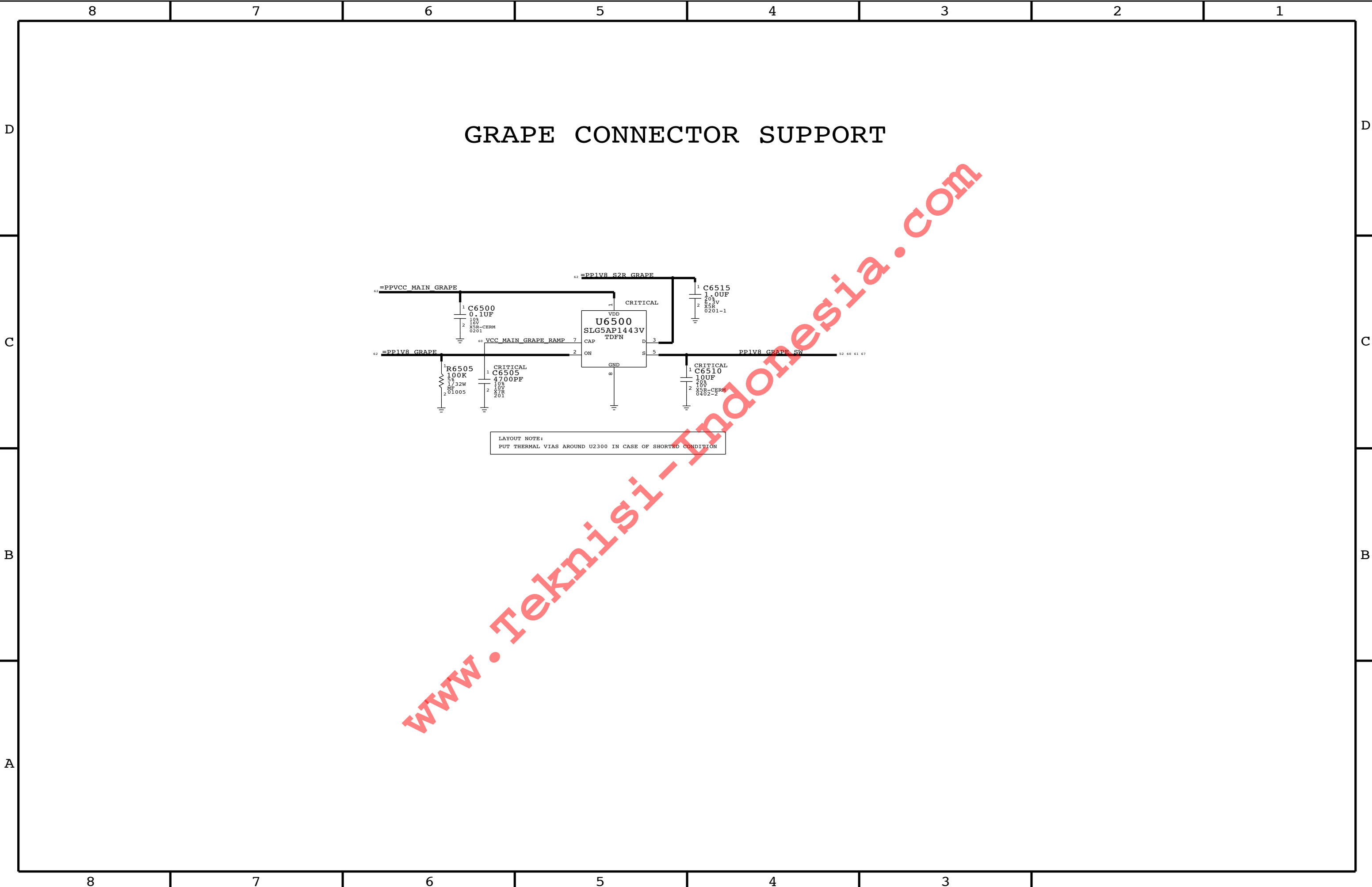




PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
377S0116	377S0108		DZ6160	RDAR:8370432
155S0320	155S0513		L6100,L6101	RDAR://PROBLEM/9625601
155S0741	155S0397		L6157	RDAR://PROBLEM/11238851



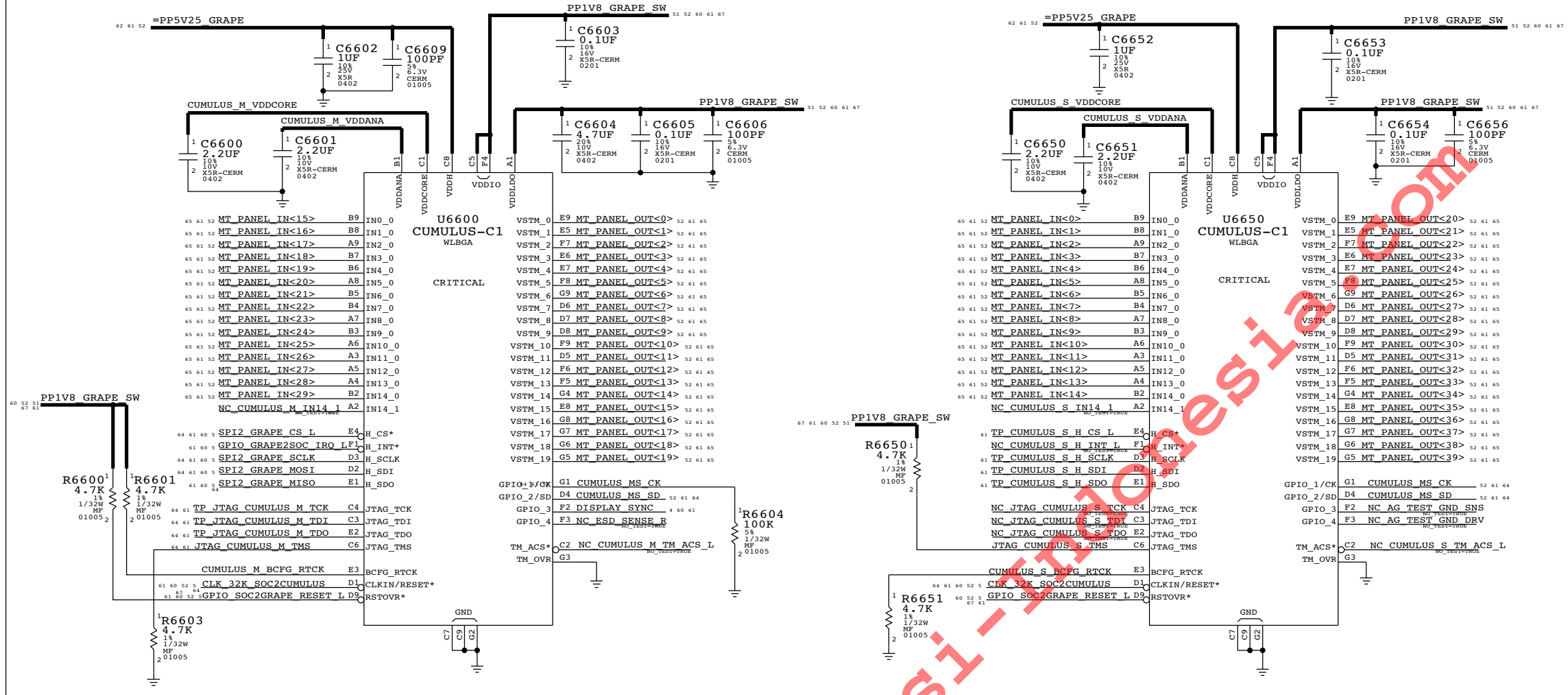




CUMULUS C1 (CSP) IN MASTER-SLAVE CONFIG

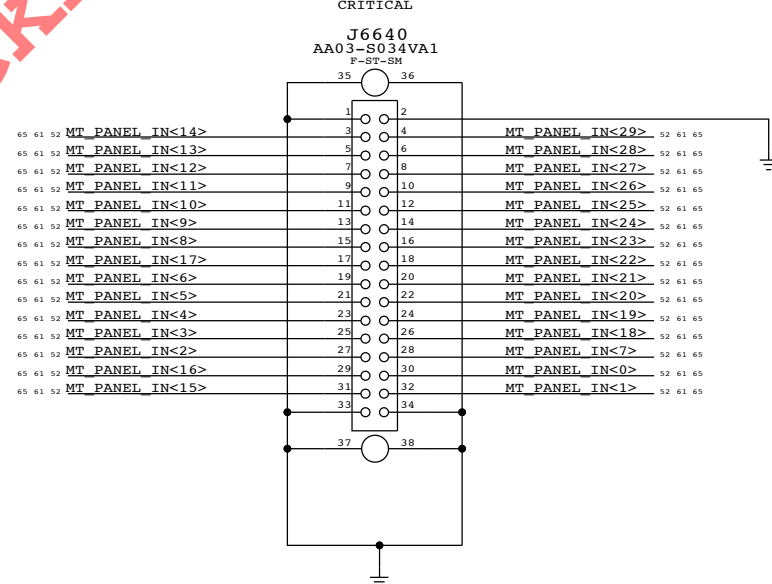
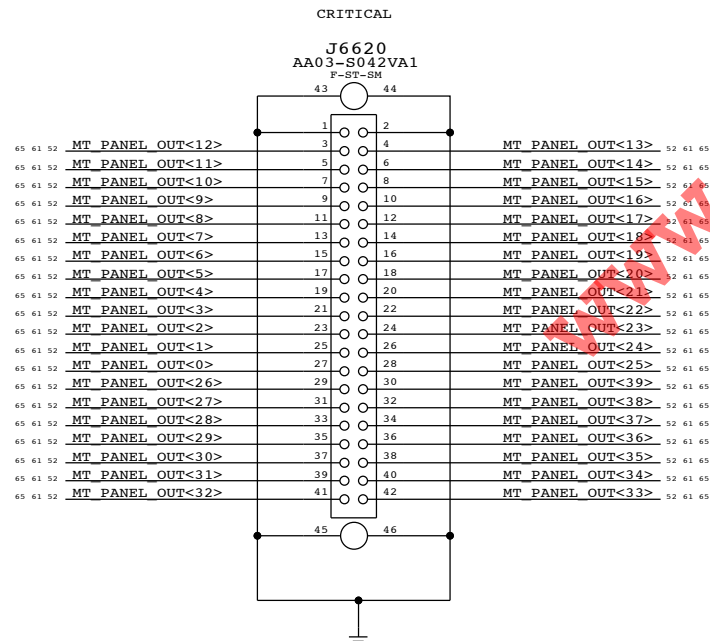
MASTER CUMULUS

SLAVE CUMULUS

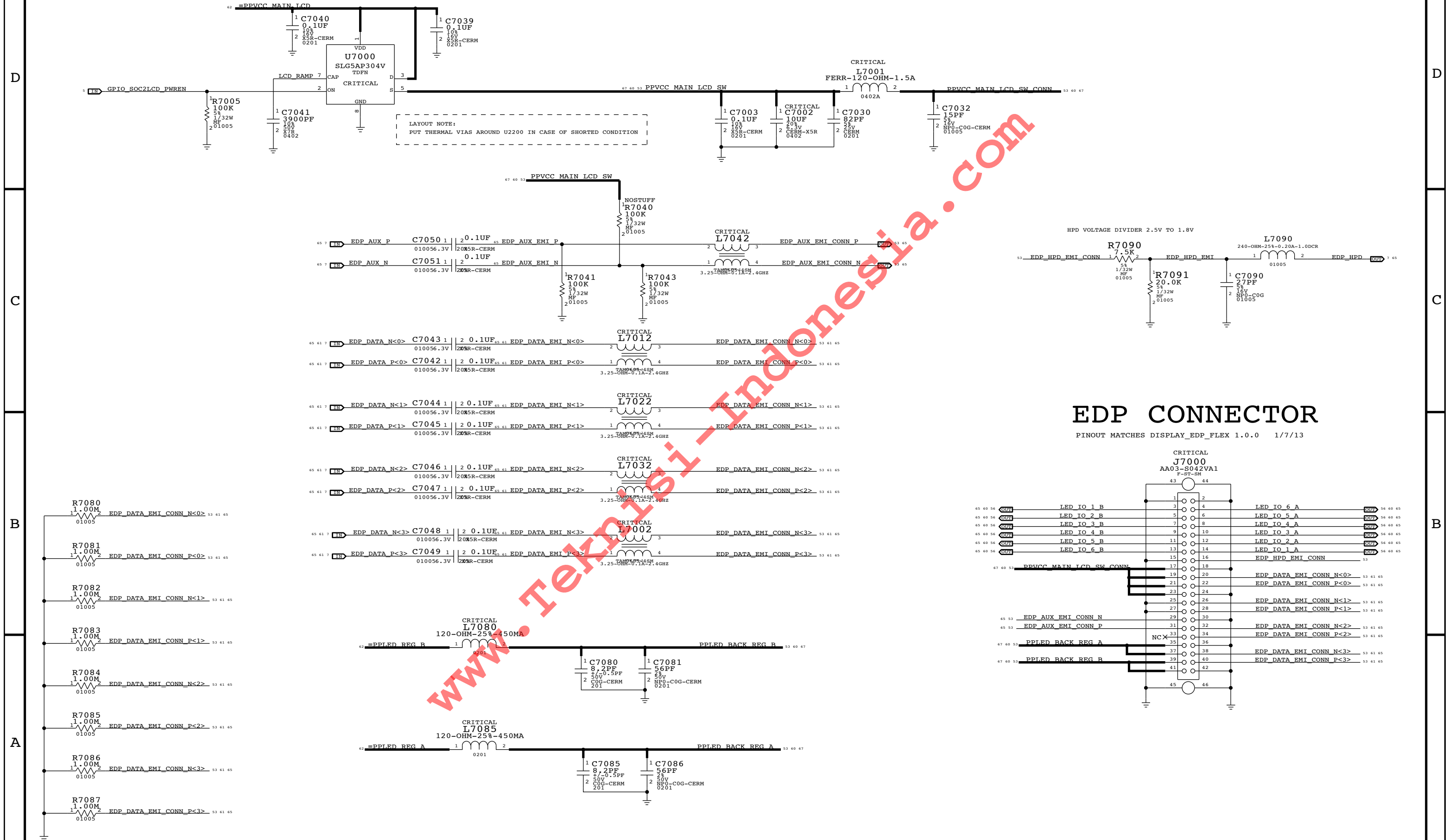


PINOUT MATCHES GRAPE_FLEX_DRIVE_ALT 0.1.0 1/8/13

PINOUT MATCHES GRAPE_FLEX_SENSE_ALT 0.1.0 1/8/13

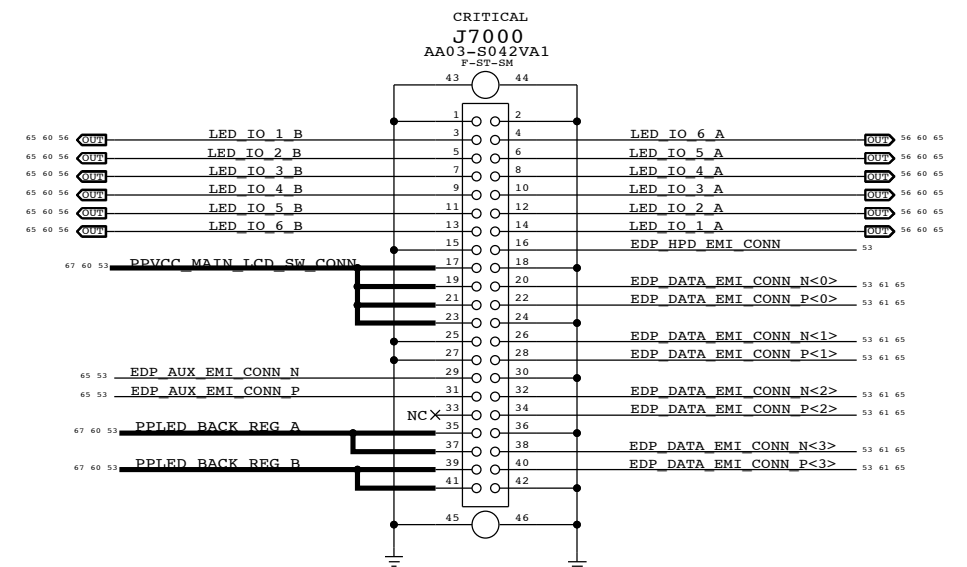


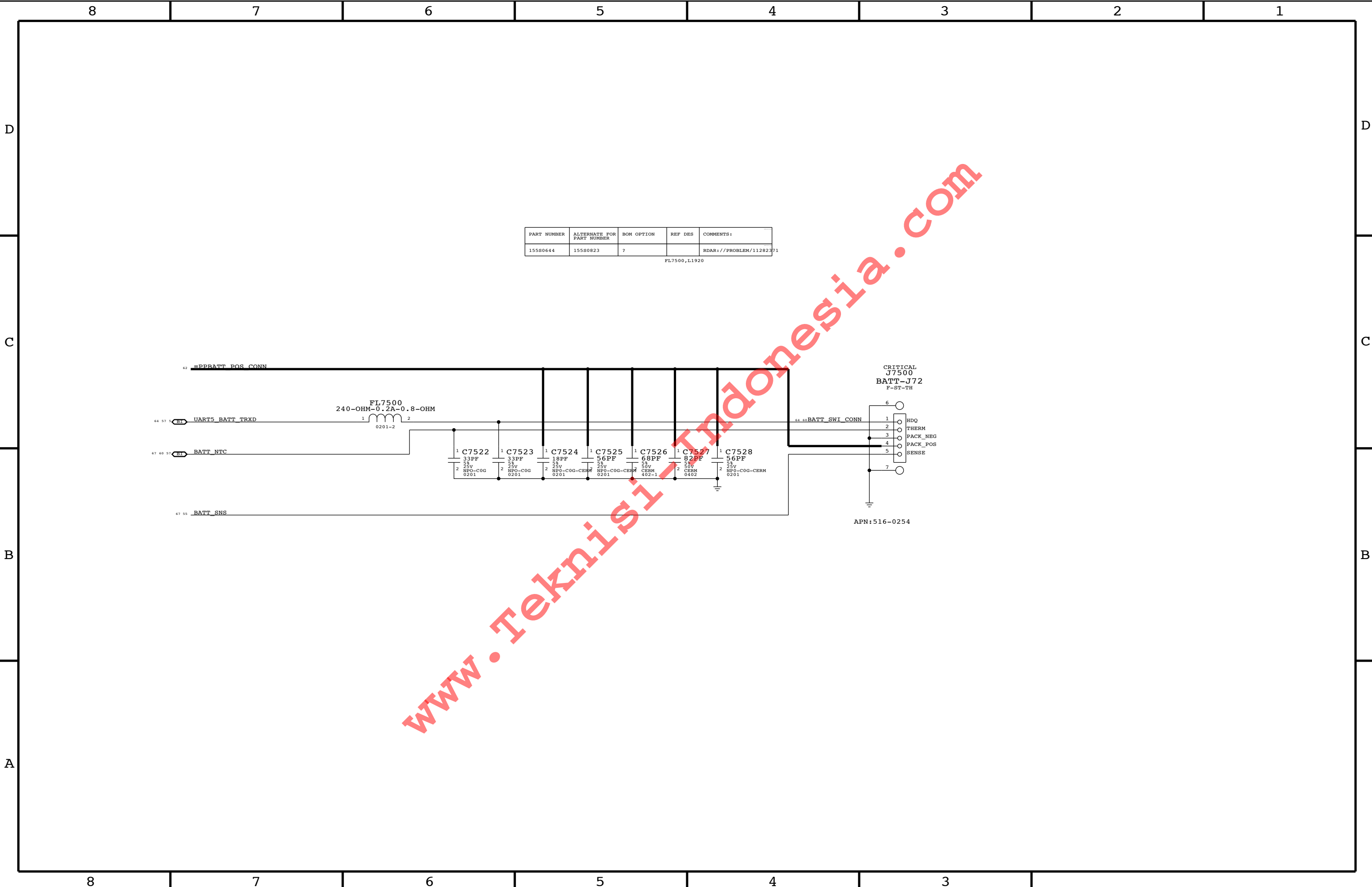
EDP CONNECTOR SUPPORT

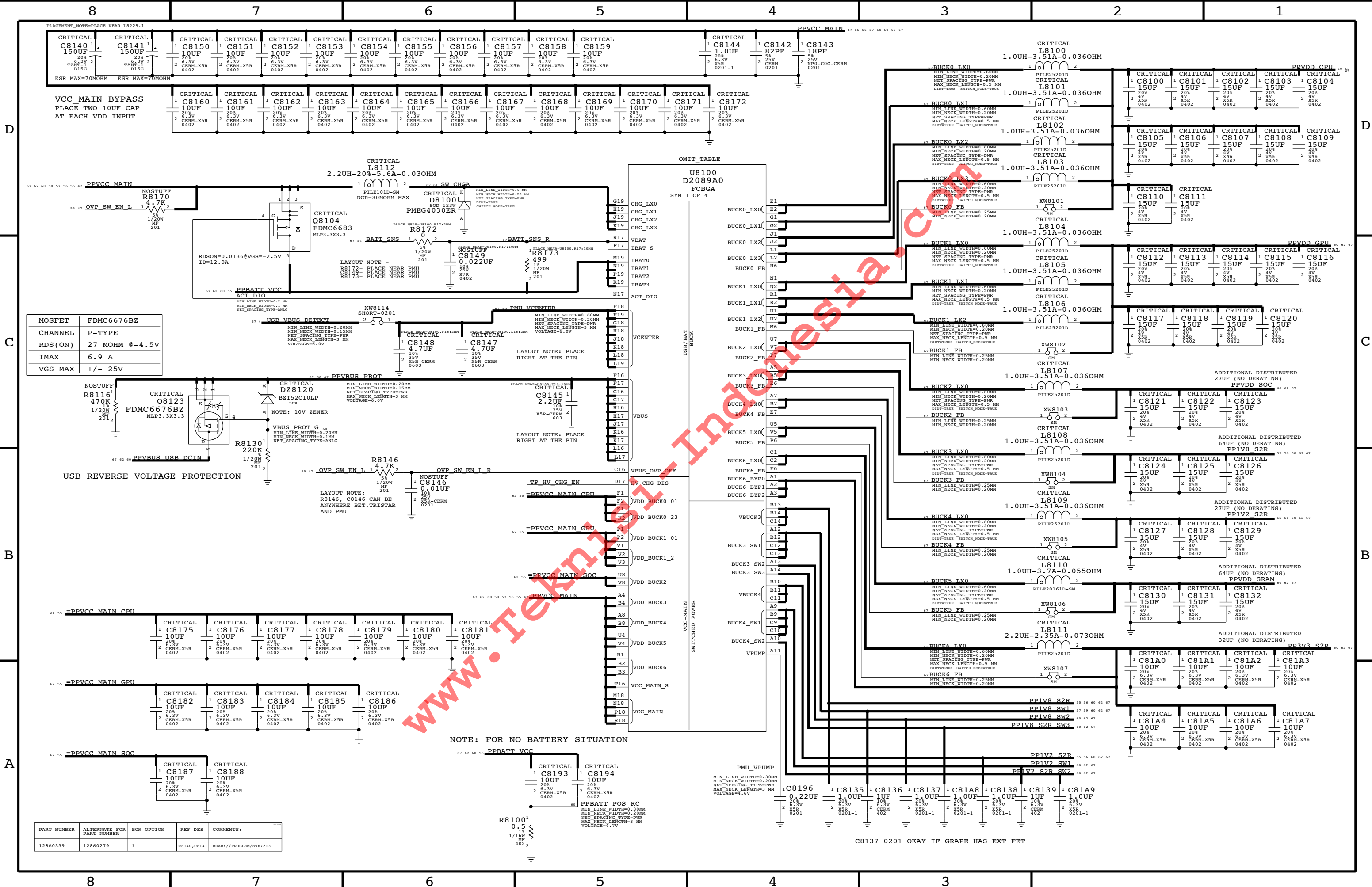


EDP CONNECTOR

PINOUT MATCHES DISPLAY_EDP_FLEX 1.0.0 1/7/13

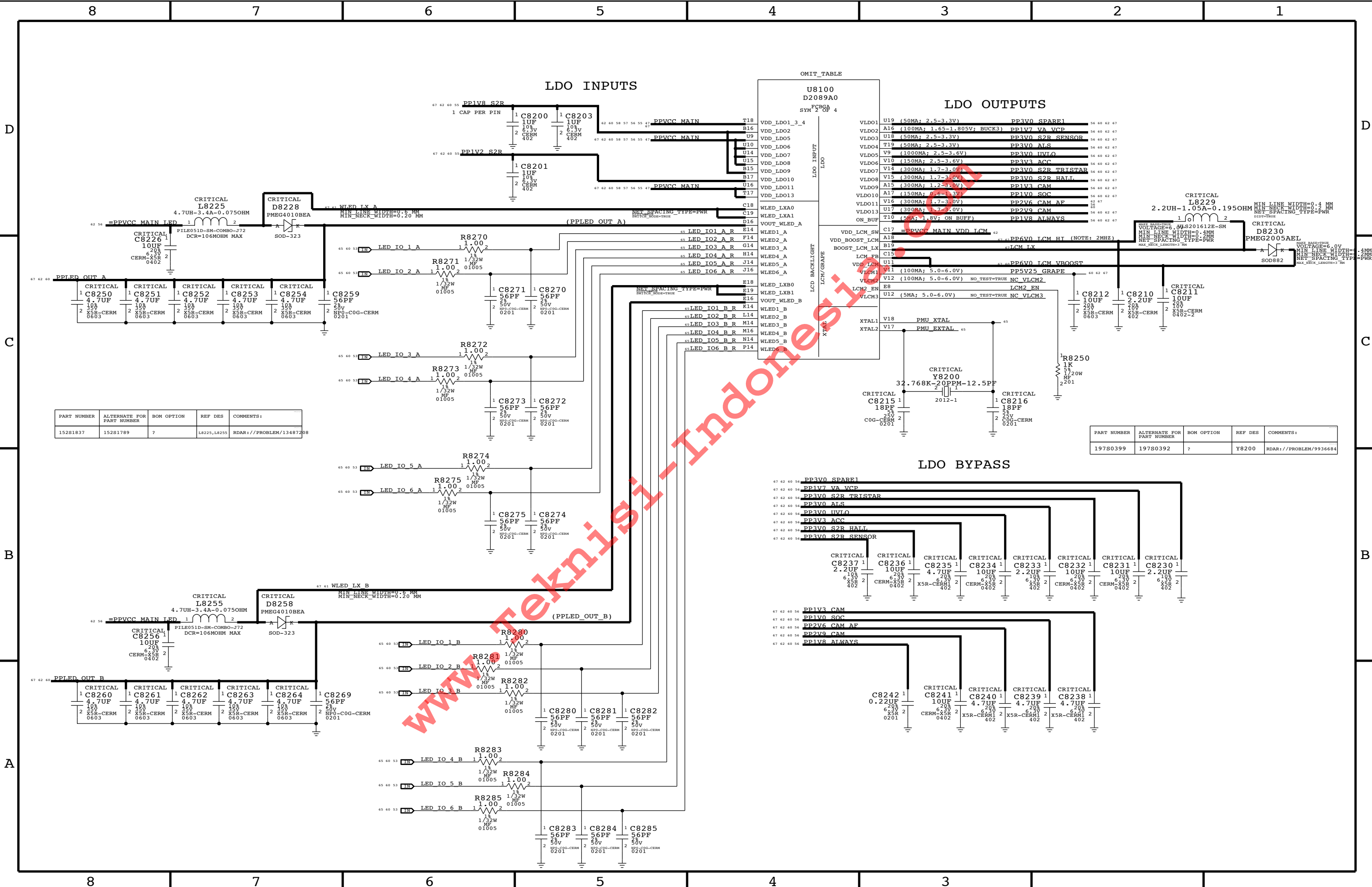






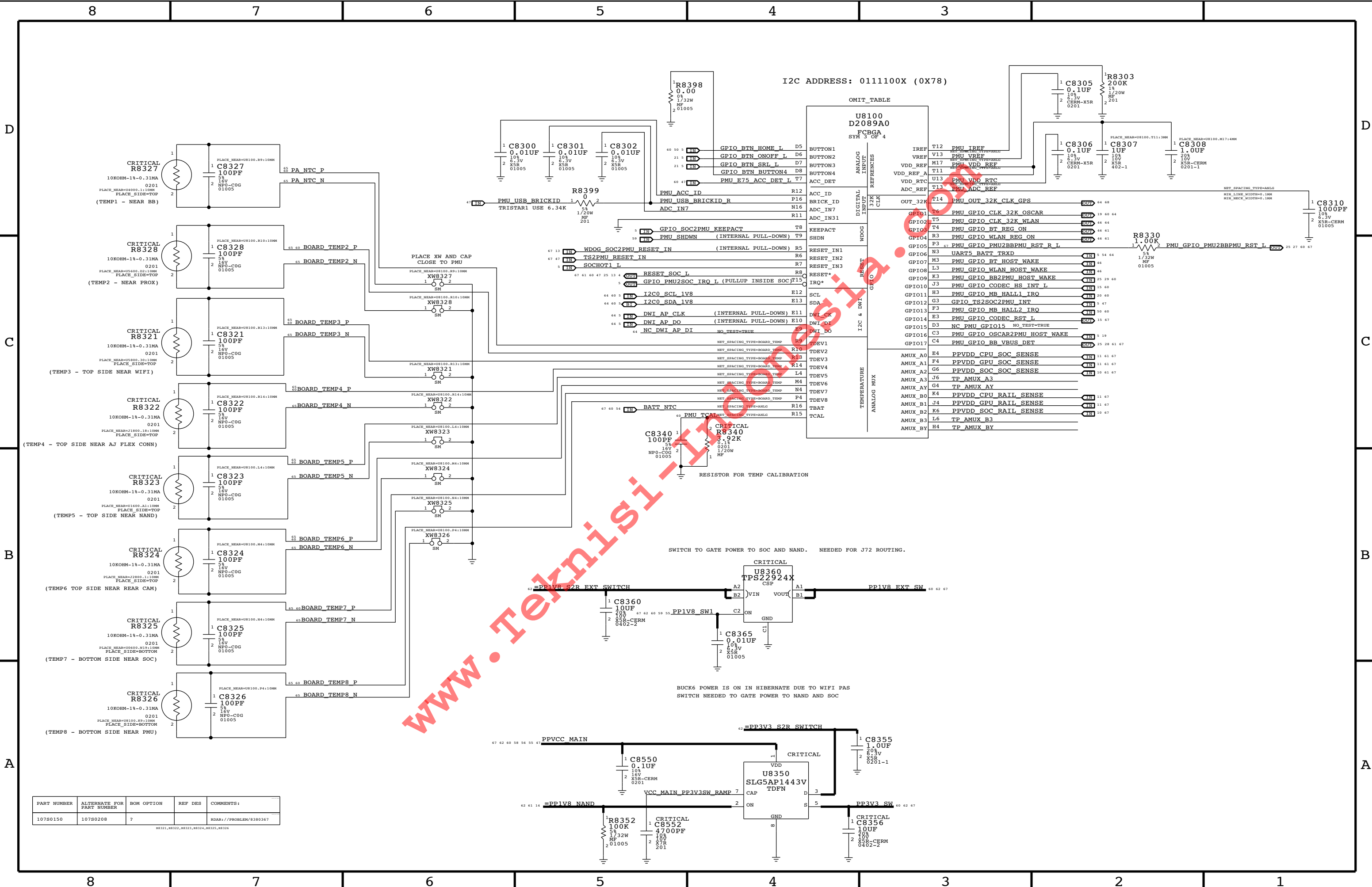
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
128S0339	128S0279	?	C8140,C8141	RDAR1//PROBLEM/8967213

C8137 0201 OKAY IF GRAPE HAS EXT FET



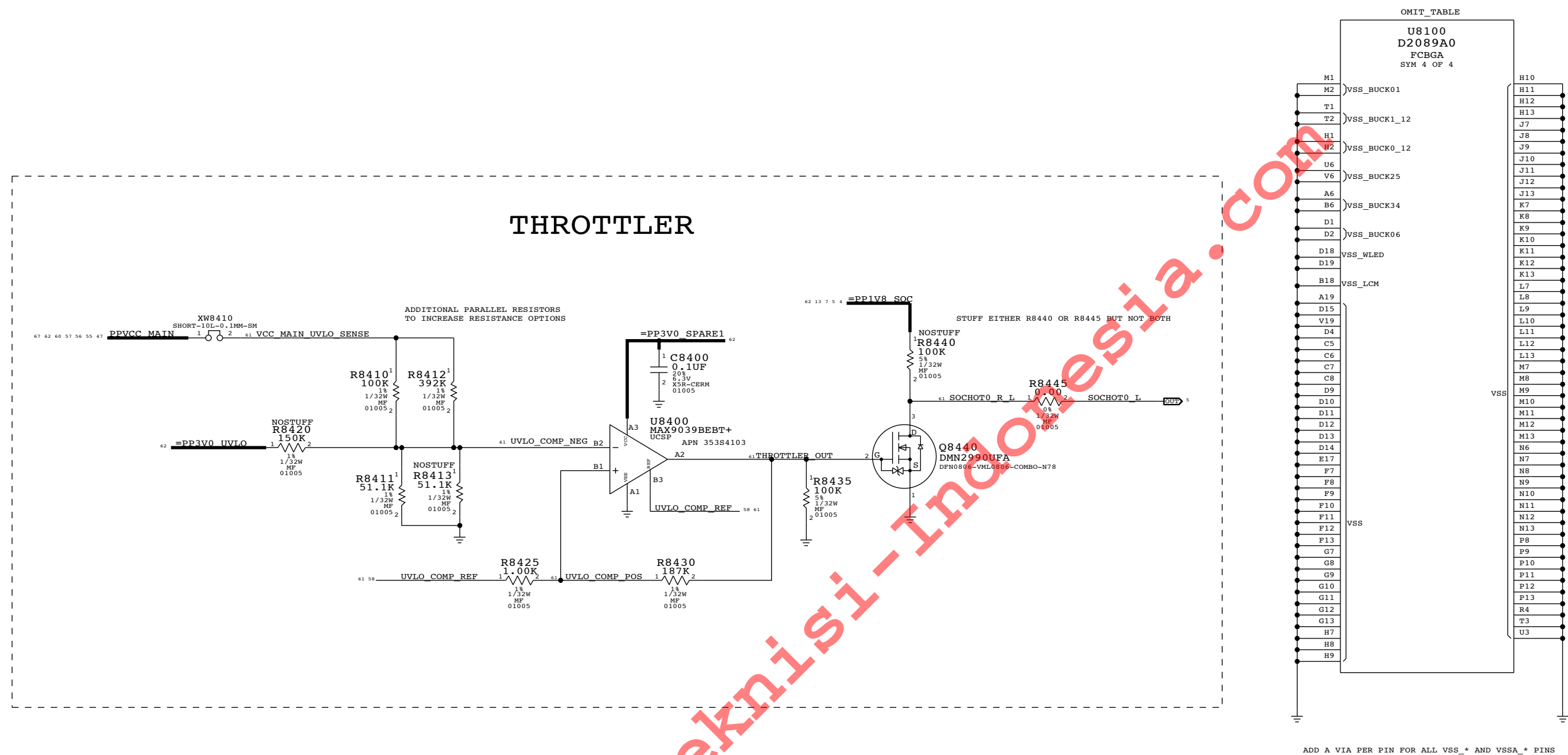
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
152S1837	152S1789	?	L8225, L8255	RDAR: //PROBLEM/13487208

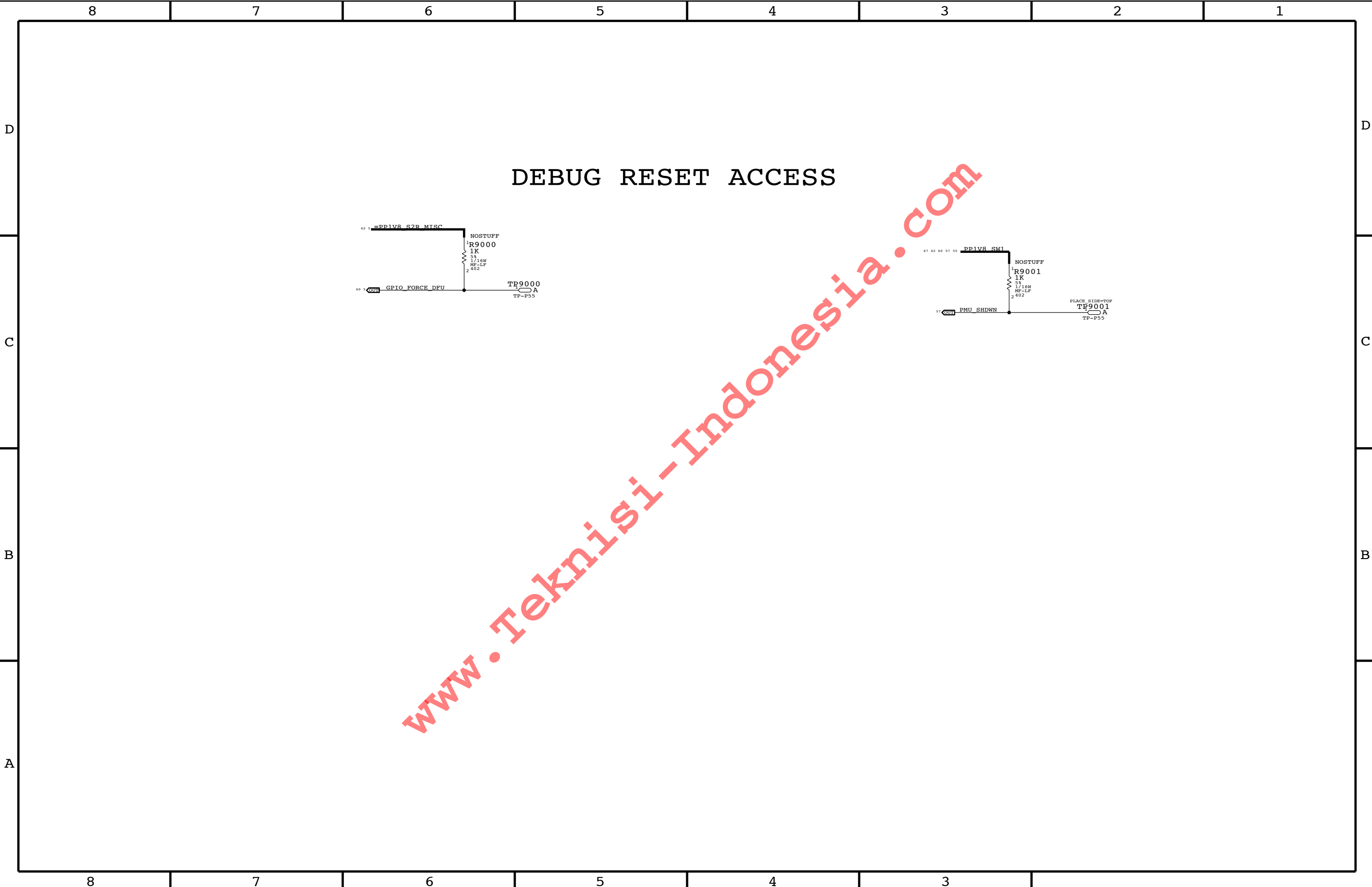
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S0399	197S0392	?	Y8200	RDAR: //PROBLEM/9936684



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
10780150	10780208	?		RDAR: // PROBLEM/8380367

R8321, R8322, R8323, R8324, R8325, R8326





EE CHARACTERIZATION TP

FOR FRANK (SEG)

NAND

BOTTOM SIDE	PP9460	1	FMI0_AD<0..7>	PLACE_SIDE=TOP	6 14 61 66
	P4MM SH	PP	NO_XNET_CONNECTION=TRUE	PLACE_NEAR=U0600.A31:2MM	
BOTTOM SIDE	PP9461	1	FMI0_DQS	PLACE_SIDE=TOP	6 14 61 66
	P4MM SH	PP	NO_XNET_CONNECTION=TRUE	PLACE_NEAR=U0600.B34:2MM	
			FMI0_AD<0..7>	EE_TEST=TRUE	6 14 61 66
			FMI0_CEO_L	FUNC_TEST=TRUE	6 14 61 66
			FMI0_ALE	FUNC_TEST=TRUE	6 14 66
			FMI0_CLE	FUNC_TEST=TRUE	6 14 66
			FMI0_WE_L	FUNC_TEST=TRUE	6 14 66
			FMI0_RE_L	FUNC_TEST=TRUE	6 14 66
			FMI0_DQS	FUNC_TEST=TRUE	6 14 61 66
			FMI1_AD<0>	FUNC_TEST=TRUE	6 14 66
			FMI1_CEO_L	FUNC_TEST=TRUE	6 14 66
			FMI1_ALE	FUNC_TEST=TRUE	6 14 66
			FMI1_CLE	FUNC_TEST=TRUE	6 14 66
			FMI1_WE_L	FUNC_TEST=TRUE	6 14 66
			FMI1_RE_L	FUNC_TEST=TRUE	6 14 66
			FMI1_DQS	FUNC_TEST=TRUE	6 14 66
			PPVREF_FMI_SOC	FUNC_TEST=TRUE	6 66
			PPVREF_FMI_NAND	FUNC_TEST=TRUE	14 66
TOP SIDE	PP9440	1	TP_FMI_TCKC_NAND	PLACE_SIDE=TOP	14
TOP SIDE	PP9441	1	TP_FMI_TMISC_NAND	PLACE_SIDE=TOP	14
TOP SIDE	PP9442	1	=PP1V8_NAND	PLACE_SIDE=TOP	14 57 62
TOP SIDE	PP9443	1	GND	PLACE_SIDE=TOP	
TOP SIDE	PP9450	1	RESET SOC_L	EE	4 13 25 47 57 60 67
	P4MM SH	PP			
TOP SIDE	PP9451	1	TP_ANALOGMUXOUT		4
	P4MM SH	PP			
TOP SIDE	PP9452	1	SOCHOTO_R_L		58
	P4MM SH	PP			
			TP_GPIO_DFU_STATUS	FUNC_TEST=TRUE	5

CAMERA

PP9470	1	MIP10C_CAM_FRONT_CLK_P	PLACE_NEAR=U0600.AM35:3MM	7 22 61 65
P4MM SH	PP	NO_XNET_CONNECTION=TRUE		
PP9471	1	MIP10C_CAM_FRONT_CLK_N	PLACE_NEAR=U0600.AM36:3MM	7 22 61 65
P4MM SH	PP	NO_XNET_CONNECTION=TRUE		
PP9472	1	MIP10C_CAM_FRONT_DATA_P<0>	PLACE_NEAR=U0600.AM35:3MM	7 22 61 65
P4MM SH	PP	NO_XNET_CONNECTION=TRUE		
PP9473	1	MIP10C_CAM_FRONT_DATA_N<0>	PLACE_NEAR=U0600.AM36:3MM	7 22 61 65
P4MM SH	PP	NO_XNET_CONNECTION=TRUE		
PP9474	1	MIP10C_CAM_REAR_CLK_P	PLACE_NEAR=U0600.AM31:3MM	7 23 61 65
P4MM SH	PP	NO_XNET_CONNECTION=TRUE		
PP9475	1	MIP10C_CAM_REAR_CLK_N	PLACE_NEAR=U0600.AM31:3MM	7 23 61 65
P4MM SH	PP	NO_XNET_CONNECTION=TRUE		
PP9476	1	MIP10C_CAM_REAR_DATA_P<0>	PLACE_NEAR=U0600.AM33:3MM	7 23 61 65
P4MM SH	PP	NO_XNET_CONNECTION=TRUE		
PP9477	1	MIP10C_CAM_REAR_DATA_N<0>	PLACE_NEAR=U0600.AM33:3MM	7 23 61 65
P4MM SH	PP	NO_XNET_CONNECTION=TRUE		

HIGH SPEED, NO TEST

		DDR0_CA<0..9>	NO_TEST=TRUE	8 12 61 66
		DDR0_CK_P	NO_TEST=TRUE	8 12 61 66
		DDR0_CK_N	NO_TEST=TRUE	8 12 61 66
		DDR0_CA<0..9>	NO_TEST=TRUE	8 12 61 66
		DDR0_CKE<0..1>	NO_TEST=TRUE	8 12 61 66
		DDR0_CSN<0..1>	NO_TEST=TRUE	8 12 66
		DDR0_DM<0..3>	NO_TEST=TRUE	8 12 66
		DDR0_DQ<0..31>	NO_TEST=TRUE	8 12 61 66
		DDR0_DQS_P<0..3>	NO_TEST=TRUE	8 12 61 66
		DDR0_DQS_N<0..3>	NO_TEST=TRUE	8 12 61 66
		DDR1_CA<0..9>	NO_TEST=TRUE	8 12 61 66
		DDR1_CK_P	NO_TEST=TRUE	8 12 61 66
		DDR1_CK_N	NO_TEST=TRUE	8 12 61 66
		DDR1_CA<0..9>	NO_TEST=TRUE	8 12 61 66
		DDR1_CKE<0..1>	NO_TEST=TRUE	8 12 61 66
		DDR1_CSN<0..1>	NO_TEST=TRUE	8 12 61 66
		DDR1_DM<0..3>	NO_TEST=TRUE	8 12 66
		DDR1_DQ<0..31>	NO_TEST=TRUE	8 12 66
		DDR1_DQS_P<0..3>	NO_TEST=TRUE	8 12 66
		DDR1_DQS_N<0..3>	NO_TEST=TRUE	8 12 66
		MIP10C_CAM_REAR_CLK_P	NO_TEST=TRUE	7 23 61 65
		MIP10C_CAM_REAR_CLK_N	NO_TEST=TRUE	7 23 61 65
		MIP10C_CAM_REAR_DATA_P<0..1>	NO_TEST=TRUE	7 23 61 65
		MIP10C_CAM_REAR_DATA_N<0..1>	NO_TEST=TRUE	7 23 61 65
		MIP10C_CAM_REAR_CLK_FILT_P	NO_TEST=TRUE	23 65
		MIP10C_CAM_REAR_CLK_FILT_N	NO_TEST=TRUE	23 65
		MIP10C_CAM_REAR_DATA_FILT_P<0..3>	NO_TEST=TRUE	23 65
		MIP10C_CAM_REAR_DATA_FILT_N<0..3>	NO_TEST=TRUE	23 65
		MIP10C_CAM_FRONT_CLK_P	NO_TEST=TRUE	7 22 61 65
		MIP10C_CAM_FRONT_CLK_N	NO_TEST=TRUE	7 22 61 65
		MIP10C_CAM_FRONT_DATA_P<0>	NO_TEST=TRUE	7 22 61 65
		MIP10C_CAM_FRONT_DATA_N<0>	NO_TEST=TRUE	7 22 61 65
		MIP10C_CAM_FRONT_CLK_FILT_P	NO_TEST=TRUE	22 65
		MIP10C_CAM_FRONT_CLK_FILT_N	NO_TEST=TRUE	22 65
		MIP10C_CAM_FRONT_DATA_FILT_P<0>	NO_TEST=TRUE	22 65
		MIP10C_CAM_FRONT_DATA_FILT_N<0>	NO_TEST=TRUE	22 65
		EDP_DATA_P<0..3>	NO_TEST=TRUE	7 53 65
		EDP_DATA_N<0..3>	NO_TEST=TRUE	7 53 65
		EDP_DATA_EMI_P<0..3>	NO_TEST=TRUE	53 65
		EDP_DATA_EMI_N<0..3>	NO_TEST=TRUE	53 65
		EDP_DATA_EMI_CONN_P<0..3>	NO_TEST=TRUE	53 65
		EDP_DATA_EMI_CONN_N<0..3>	NO_TEST=TRUE	53 65

DRAM

NEAR DRAM

PP9410	1	DDR0_CK_N	PLACE_NEAR=U1400.AF14:1MM	8 12 61 66
P4MM SH	PP	NO_XNET_CONNECTION=TRUE		
PP9411	1	DDR0_CK_P	PLACE_NEAR=U1400.AF15:1MM	8 12 61 66
P4MM SH	PP	NO_XNET_CONNECTION=TRUE		
PP9412	1	DDR0_CKE<0>	PLACE_NEAR=U1400.AF16:1MM	8 12 61 66
P4MM SH	PP	NO_XNET_CONNECTION=TRUE		
PP9413	1	DDR0_CKE<1>	PLACE_NEAR=U1400.AE17:1MM	8 12 61 66
P4MM SH	PP	NO_XNET_CONNECTION=TRUE		
PP9414	1	DDR0_CA<0>	PLACE_NEAR=U1400.AE21:1MM	8 12 61 66
P4MM SH	PP	NO_XNET_CONNECTION=TRUE		
PP9415	1	DDR0_DQ<2>	PLACE_NEAR=U1400.B18:1MM	8 12 61 66
P4MM SH	PP	NO_XNET_CONNECTION=TRUE		
PP9416	1	DDR0_DQS_N<3>	PLACE_NEAR=U1400.C8:1MM	8 12 61 66
P4MM SH	PP	NO_XNET_CONNECTION=TRUE		
PP9417	1	DDR0_DQS_P<3>	PLACE_NEAR=U1400.B8:1MM	8 12 61 66
P4MM SH	PP	NO_XNET_CONNECTION=TRUE		
PP9418	1	DDR0_DQS_N<0>	PLACE_NEAR=U1400.C15:1MM	8 12 61 66
P4MM SH	PP	NO_XNET_CONNECTION=TRUE		
PP9419	1	DDR0_DQS_P<0>	PLACE_NEAR=U1400.B15:1MM	8 12 61 66
P4MM SH	PP	NO_XNET_CONNECTION=TRUE		
PP9420	1	DDR1_CK_N	PLACE_NEAR=U1400.T26:1MM	8 12 61 66
P4MM SH	PP	NO_XNET_CONNECTION=TRUE		
PP9421	1	DDR1_CK_P	PLACE_NEAR=U1400.R26:1MM	8 12 61 66
P4MM SH	PP	NO_XNET_CONNECTION=TRUE		
PP9422	1	DDR1_CKE<0>	PLACE_NEAR=U1400.P26:1MM	8 12 61 66
P4MM SH	PP	NO_XNET_CONNECTION=TRUE		
PP9423	1	DDR1_CKE<1>	PLACE_NEAR=U1400.N25:1MM	8 12 61 66
P4MM SH	PP	NO_XNET_CONNECTION=TRUE		
PP9424	1	DDR1_CA<0>	PLACE_NEAR=U1400.J25:1MM	8 12 61 66
P4MM SH	PP	NO_XNET_CONNECTION=TRUE		
PP9425	1	DDR1_CA<1>	PLACE_NEAR=U1400.K26:1MM	8 12 61 66
P4MM SH	PP	NO_XNET_CONNECTION=TRUE		
PP9426	1	DDR1_CA<2>	PLACE_NEAR=U1400.K25:1MM	8 12 61 66
P4MM SH	PP	NO_XNET_CONNECTION=TRUE		
PP9427	1	DDR1_CA<3>	PLACE_NEAR=U1400.L25:1MM	8 12 61 66
P4MM SH	PP	NO_XNET_CONNECTION=TRUE		
PP9428	1	DDR1_CSN<0>	PLACE_NEAR=U1400.N35:1MM	8 12 61 66
P4MM SH	PP	NO_XNET_CONNECTION=TRUE		

NEAR SOC

PP9435	1	DDR0_DQ<28>	PLACE_NEAR=U0600.D5:1MM	8 12 61 66
P4MM SH	PP	NO_XNET_CONNECTION=TRUE		
PP9436	1	DDR0_DQS_N<3>	PLACE_NEAR=U0600.A6:1MM	8 12 61 66
P4MM SH	PP	NO_XNET_CONNECTION=TRUE		
PP9437	1	DDR0_DQS_P<3>	PLACE_NEAR=U0600.A5:1MM	8 12 61 66
P4MM SH	PP	NO_XNET_CONNECTION=TRUE		
		PP6V0_LCM_HI	NO_TEST=TRUE	56 67
		SW_CHGA	NO_TEST=TRUE	56 67
		WLED_LX_A	NO_TEST=TRUE	56 67
		WLED_LX_B	NO_TEST=TRUE	56 67
		L81_PVCP	NO_TEST=TRUE	15 65
		L81_NVCP	NO_TEST=TRUE	15 65
		CHARGE_PUMP_OUTPUTS	NO_TEST=TRUE	15 65
		L81_FLYC	NO_TEST=TRUE	15 65
		L81_FLYN	NO_TEST=TRUE	15 65
		L81_FLYP	NO_TEST=TRUE	15 65
		THROTTLE_OUT	NO_TEST=TRUE	58
		UVLO_COMP_NEG	NO_TEST=TRUE	58
		UVLO_COMP_POS	NO_TEST=TRUE	58
		UVLO_COMP_REF	NO_TEST=TRUE	58
		VCC_MAIN_UVLO_SENSE	NO_TEST=TRUE	58

POWER, NO TEST

GRAPE

CONVERT TO PROBE POINTS IF NOT ABLE TO PLACE TESTPOINT

5262	TP JTAG CUMULUS M TCK	52 64
5263	TP JTAG CUMULUS M TDI	52 64
5264	JTAG CUMULUS M TMS	52 64
5265	TP JTAG CUMULUS M TDO	52 64
5266	DISPLAY SYNC	52 64
5267	CUMULUS_MS_CK	52 64
5268	CUMULUS_MS_SD	52 64
5269	GPIO GRAPE2SOC IRQ L	5 52 60
5270	GPIO SOC2GRAPE RESET L	5 52 60 67
5271	CLK 32K SOC2CUMULUS	5 52 60 64
5272	SPI2 GRAPE MOSI	5 52 60 64
5273	SPI2 GRAPE MISO	5 52 60 64
5274	SPI2 GRAPE SCLK	5 52 60 64
5275	SPI2 GRAPE CS L	5 52 60 64
5276	TP CUMULUS_S_H_CS_L	52
5277	TP CUMULUS_S_H_SCLK	52
5278	TP CUMULUS_S_H_SDI	52
5279	TP CUMULUS_S_H_SDO	52
5280	=PP5V25_GRAPE	52 62
5281	PP1V8_GRAPE_SW	51 52 60 67
5282	GRAPE_NO_TEST	
5283	MT_PANEL_IN<0..29>	NO_TEST=TRUE 52 65
5284	MT_PANEL_OUT<0..39>	NO_TEST=TRUE 52 65

AUDIO

		L81_DMIC1_FF_SD	FUNC_TEST=TRUE	15
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NO TEST DUE TO LAYOUT

		I2C3_TP_AT_ALS_FILTER_SIDE		
		I2C3_SCL_1V8	NO_TEST=TRUE	5 13 22 64
		I2C3_SDA_1V8	NO_TEST=TRUE	5 13 22 64
		MAX98304_L1_IN_N	NO_TEST=TRUE	18 65
		MAX98304_L1_IN_P	NO_TEST=TRUE	18 65
		MAX98304_R1_IN_N	NO_TEST=TRUE	17 65
		MAX98304_R1_IN_P	NO_TEST=TRUE	17 65
		MAX98304_L2_IN_N	NO_TEST=TRUE	18 65
		MAX98304_L2_IN_P	NO_TEST=TRUE	18 65
		MAX98304_R2_IN_N	NO_TEST=TRUE	17 65
		MAX98304_R2_IN_P	NO_TEST=TRUE	17 65
		GPIO_BTN_HOME_CONN_R_L	NO_TEST=TRUE	50

NO TEST ON PROX

		PROX_AD7149_CIN5	NO_TEST=TRUE	45
		PROX_AD7149_CIN7	NO_TEST=TRUE	45
		PROX_AD7149_CIN9	NO_TEST=TRUE	45
		PROX_AD7149_CIN7_FILT	NO_TEST=TRUE	45
		PROX_AD7149_CIN9_FILT	NO_TEST=TRUE	45
		PROX_AD7149_CIN7_CONN	NO_TEST=TRUE	45
		PROX_AD7149_CIN9_CONN	NO_TEST=TRUE	45
		PROX_AD7149_ACSHIELD_CONN	NO_TEST=TRUE	45
		PROX_AD7149_BIAS	NO_TEST=TRUE	45
		ACSHIELD_SB	NO_TEST=TRUE	45
		ACSH_SB	NO_TEST=TRUE	45
		PROX_AD7149_GPIO	NO_TEST=TRUE	45

WIFI

		JTAG_WLAN_TMS_TX_BLANK	FUNC_TEST=TRUE	46 64
		TP_JTAG_WLAN_TCK	FUNC_TEST=TRUE	46 64
		JTAG_WLAN_TDI_OSCAR_A	FUNC_TEST=TRUE	46 64
		JTAG_WLAN_TDO_OSCAR_B	FUNC_TEST=TRUE	46 64
		TP_JTAG_WLAN_TRST_L	FUNC_TEST=TRUE	46 64
		JTAG_WLAN_SEL	FUNC_TEST=TRUE	46
		UART2_SOC2WLAN_TX_R	FUNC_TEST=TRUE	46 64
		UART2_WLAN2SOC_TX_R	FUNC_TEST=TRUE	46 64
		UART_BB2WLAN_LTE_COEX_R	FUNC_TEST=TRUE	46 64
		UART_WLAN2BB_LTE_COEX_R	FUNC_TEST=TRUE	46 64
		=PP3V3_S2R_WIFI_PA	FUNC_TEST=TRUE	46 62
		HSIC1_SOC2WLAN_HOST_RDY_R	FUNC_TEST=TRUE	46 64
		HSIC1_WLAN2SOC_DEVICE_RDY	FUNC_TEST=TRUE	5 46 64
		HSIC1_WLAN2SOC_REMOTE_WAKE	FUNC_TEST=TRUE	5 46 64

FOR HSIC CHARACTERIZATION

PP9480	1	HSIC1_WLAN_DATA	PLACE_NEAR=U0600.A27:3MM	4 46 61 64
P4MM SH	PP			
PP9481	1	HSIC1_WLAN_STB	PLACE_NEAR=U0600.B27:3MM	4 46 61 64
P4MM SH	PP			
PP9482	1	HSIC1_WLAN_DATA	PLACE_NEAR=U5800.13:3MM	4 46 61 64
P4MM SH	PP			
PP9483	1	HSIC1_WLAN_STB	PLACE_NEAR=U5800.14:3MM	4 46 61 64
P4MM SH	PP			
		PMU_GPIO_WLAN_REG_ON	FUNC_TEST=TRUE	46 57
		PMU_GPIO_BT_REG_ON	FUNC_TEST=TRUE	46 57
		GPIO_BT_WAKE	FUNC_TEST=TRUE	5 46

BASEBAND

		BB_JTAG_TMS	FUNC_TEST=TRUE	5 25 28 64
		BB_JTAG_TCK	FUNC_TEST=TRUE	5 25 28 64
		BB_JTAG_TDI	FUNC_TEST=TRUE	5 25 28 64
		BB_JTAG_TDO	FUNC_TEST=TRUE	5 25 28 64
		BB_JTAG_TRST_L	FUNC_TEST=TRUE	5 25 28 64
		USB_BB_DEBUG_P	FUNC_TEST=TRUE	25 28 64
		USB_BB_DEBUG_N	FUNC_TEST=TRUE	25 28 64
		DEBUG_RST_L	FUNC_TEST=TRUE	25 28 67
		PMU_GPIO_BB_VBUS_DET	FUNC_TEST=TRUE	25 28 57 67

FOR HSIC CHARACTERIZATION

PP9485	1	HSIC2_BB_DATA	PLACE_NEAR=U0600.AJ35:3MM	4 25 28 61 64
P4MM	SM			
PP9486	1	HSIC2_BB_STB	PLACE_NEAR=U0600.AJ36:3MM	4 25 28 61 64
P4MM	SM			
PP9487	1	HSIC2_BB_DATA	PLACE_NEAR=U3400.C7:3MM	4 25 28 61 64
P4MM	SM			
PP9488	1	HSIC2_BB_STB	PLACE_NEAR=U3400.B8:3MM	4 25 28 61 64
P4MM	SM			

Diagram illustrating the Power Connections for a device, organized into columns (8 to 1) and rows (A to D).

BUCK0

- PPVDD_CPU (MAKE_BASE=TRUE) connected to PPVDD_CPU (11)

BUCK1

- PPVDD_GPU (MAKE_BASE=TRUE) connected to PPVDD_GPU (11)

BUCK2

- PPVDD_SOC (MAKE_BASE=TRUE) connected to PPVDD_SOC (10)

BUCK3

- PP1V8_S2R (MAKE_BASE=TRUE) connected to PP1V8_S2R_MISC (5 59), PP1V8_S2R_VDDIO_WLAN_BT (46), PP1V8_S2R_TRISTAR (47), PP1V8_S2R_DDR (12), PP1V8_S2R_GRAPE (51), and PP1V8_S2R_EXT_SWITCH (57)

BUCK3_SW

- PP1V8_SW1 (MAKE_BASE=TRUE) connected to PP1V8_AUDIO (15) and PP1V8_SW1_FOREHEAD (60 62 67) via XWC130 SM
- PP1V8_SW1_FOREHEAD connected to PP1V8_DMIC (16), PP1V8_CAM_FRONT (22), PP1V8_CAM_REAR (23), and PP1V8_PROX_AD7149 (45)
- PP1V8_EXT_SW (MAKE_BASE=TRUE) connected to PP1V8_VDDIO18_SOC (9 10), PP1V8_SOC (4 5 7 13 58), PP1V8_MIPI_SOC (7), PP1V8_EDP_SOC (7), PP1V8_NAND_SOC (6), PP1V8_NAND (14 57 61), PP1V8_PLL_SOC (4), and PP1V8_EEPROM (5)
- PP1V8_SW2 (MAKE_BASE=TRUE) connected to PP1V8_GRAPE (51)
- PP1V8_S2R_SW3 (MAKE_BASE=TRUE) connected to PP1V8_S2R_GYRO (19), PP1V8_S2R_ACCEL (19), and PP1V8_S2R_OLSCAR (19)
- PP1V8_S2R_SW3_COMP (MAKE_BASE=TRUE) connected to PP1V8_S2R_SW3_COMP (60 62 67) via XWC133 SM and PP1V8_S2R_COMP (24)

BUCK4

- PP1V2_S2R (MAKE_BASE=TRUE) connected to PP1V2_S2R_DDR (12) and PP1V2_S2R_DDR_SOC (8)

BUCK4_SW

- PP1V2_SW1 (MAKE_BASE=TRUE) connected to PP1V2_VDDQ_DDR (12), PP1V2_VDDIOD_SOC (8 9), and PP1V2_HSIC_SOC (4)
- PP1V2_S2R_SW2 (MAKE_BASE=TRUE) connected to PP1V2_S2R_OLSCAR (19)

BUCK5

- PPVDD_SRAM (MAKE_BASE=TRUE) connected to PPVDD_SRAM_CPU (10) and PPVDD_SRAM_SOC (10)

BUCK6

- PP3V3_S2R (MAKE_BASE=TRUE) connected to PP3V3_S2R_SWITCH (57) and PP3V3_S2R_WIFI_PA (46 61)
- PP3V3_SW (MAKE_BASE=TRUE) connected to PP3V3_EDP_PU, PP3V3_NAND (14), and PP3V3_USB_SOC (4)

LDO1

- PP3V0_SPARE1 (MAKE_BASE=TRUE) connected to PP3V0_SPARE1 (58)

LDO2

- PP1V7_VA_VCP (MAKE_BASE=TRUE) connected to PP1V7_VA_VCP (15)

LDO3

- PP3V0_S2R_SENSOR (MAKE_BASE=TRUE) connected to PP3V0_S2R_GYRO (19), PP3V0_S2R_ACCEL (19), and PP3V0_S2R_COMP (24)

LDO4

- PP3V0_ALS (MAKE_BASE=TRUE) connected to PP3V0_ALS (22) and PP3V0_PROX_AD7149 (45)

LDO5

- PP3V0_UVLO (MAKE_BASE=TRUE) connected to PP3V0_UVLO (58)

LDO6

- PP3V3_ACC (MAKE_BASE=TRUE) connected to PP3V3_ACC (47)

LDO7

- PP3V0_S2R_TRISTAR (MAKE_BASE=TRUE) connected to PP3V0_S2R_TRISTAR (47)

LDO8

- PP3V0_S2R_HALL (MAKE_BASE=TRUE) connected to PP3V0_S2R_HALL (50)

LDO9

- PP1V3_CAM (MAKE_BASE=TRUE) connected to PP1V3_CAM_REAR (23)

LDO10

- PP1V0_SOC (MAKE_BASE=TRUE) connected to PP1V0_USB_SOC (4), PP1V0_MIPI_SOC (7), and PP1V0_EDP_PAD_DVDD_SOC (7)

LDO11

- PP2V6_CAM_AF (MAKE_BASE=TRUE) connected to PP2V6_CAM_REAR_AF (23)

LDO13

- PP2V9_CAM (MAKE_BASE=TRUE) connected to PP2V9_CAM_FRONT (22) and PP2V9_CAM_REAR (23)

VLCM1

- PP5V25_GRAPE (MAKE_BASE=TRUE) connected to PP5V25_GRAPE (52 61)

CHARGER MAIN

- PPVCC_MAIN (MAKE_BASE=TRUE) connected to PPVCC_MAIN_AUDIO (15), PPVCC_MAIN_LED (56), PPVCC_MAIN_CPU (55), PPVCC_MAIN_GPU (55), PPVCC_MAIN_SOC (55), PPVCC_MAIN_GRAPE (51), PPVCC_MAIN_LCD (53), PPVCC_MAIN_VDD_LCM (56), and PPVCC_MAIN_WLAN (46)

BATTERY

- PPBATT_VCC (MAKE_BASE=TRUE) connected to PPBATT_POS_CONN (54), PPBATT_VCC_BB (25 26 34 35 36 37 38 39 40), and PPBATT_AUDIO (17 18)

USB POWER INPUT

- PPVBUS_USB_DCIN (MAKE_BASE=TRUE) connected to PPVBUS_USB_EMI (48)

ON_BUF

- PP1V8_ALWAYS (MAKE_BASE=TRUE) connected to PP1V8_ALWAYS (5)

BACKLIGHT BOOST

- PPLED_OUT_A (MAKE_BASE=TRUE) connected to PPLED_REG_A (53)
- PPLED_OUT_B (MAKE_BASE=TRUE) connected to PPLED_REG_B (53)

D

C

B

Clock Signal Constraints

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET	NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_50S	*	45_OHM_SE	CLK	*	*	3:1_SPACING

ELECTRICAL_CONSTRAINT_SET		NET_TYPE		PHYSICAL	SPACING	
525		CLK_50S	CLK	CLK 32K SOC2CUMULUS		5 52 60 61
526		CLK_50S	CLK	CLK 32K SOC2CUMULUS FILT		60
527		CLK_50S	CLK	CUMULUS MS CK		52 61
528		CLK_50S	CLK	CUMULUS MS_SD		52 61
529		CLK_50S	CLK	PMU GPIO CLK 32K WLAN		46 57
530		CLK_50S	CLK	PMU GPIO CLK 32K OSCAR		19 57 60
531		CLK_50S	CLK	PMU OUT 32K CLK GPS		57 68
532		CLK_50S	CLK	ISPI CAM FRONT CLK R		7
533		CLK_50S	CLK	ISPI CAM FRONT CLK		7 22
534		CLK_50S	CLK	ISPI CAM FRONT CLK F		22 60
535		CLK_50S	CLK	ISPO CAM REAR CLK R		7
536		CLK_50S	CLK	ISPO CAM REAR CLK		7 23
537		CLK_50S	CLK	ISPO CAM REAR CLK F		23 60

UART

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET	NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
UART_50S	*	45_OHM_SE	UART	*	*	3:1_SPACING
			UART	UART	*	2:1_SPACING

ELECTRICAL_CONSTRAINT_SET		NET_TYPE		PHYSICAL	SPACING	
538		UART_50S	UART	UART0 SOC_RXD		5 47 60
539		UART_50S	UART	UART0 SOC_TXD		5 47 60
540		UART_50S	UART	UART3 SOC2BB_RTS_L		5 25 29
541		UART_50S	UART	UART3 BB2SOC_RTS_L		5 25 29
542		UART_50S	UART	UART3 SOC2BB_TX		5 25 29 47
543		UART_50S	UART	UART3 BB2SOC_TX		5 25 29 47
544		UART_50S	UART	UART4 OSCAR2SOC_RXD		5 19
545		UART_50S	UART	UART4 SOC2OSCAR_TXD		5 19
546		UART_50S	UART	UART1 SOC2BT_RTS_L		5 46
547		UART_50S	UART	UART1 BT2SOC_RTS_L		5 46
548		UART_50S	UART	UART1 SOC2BT_TX		5 46
549		UART_50S	UART	UART1 BT2SOC_TX		5 46
550		UART_50S	UART	UART2 SOC2WLAN_TX		5 46
551		UART_50S	UART	UART2 WLAN2SOC_TX		5 46
552		UART_50S	UART	UART2 SOC2WLAN_TX_R		46 61
553		UART_50S	UART	UART2 WLAN2SOC_TX_R		46 61
554		UART_50S	UART	UART6 TS_ACC_RXD		5 47
555		UART_50S	UART	UART6 TS_ACC_TXD		5 47
556			UART	UART5 BATT_TRXD		5 54 57
557			UART	BATT_SWI_CONN		54 60

I2S

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET	NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
I2S_50S	*	45_OHM_SE	I2S	*	*	3:1_SPACING
			I2S	I2S	*	2:1_SPACING

ELECTRICAL_CONSTRAINT_SET		NET_TYPE		PHYSICAL	SPACING	
558		I2S_50S	CLK	I2S0 CODEC ASP_MCK_R		5 15
559		I2S_50S	CLK	I2S0 CODEC ASP_MCK		5
560		I2S_50S	I2S	I2S0 CODEC ASP_BCLK		5 15
561		I2S_50S	I2S	I2S0 CODEC ASP_LRCK		5 15
562		I2S_50S	I2S	I2S0 CODEC ASP_DIN		5 15
563		I2S_50S	I2S	I2S0 CODEC ASP_DOUT		5 15
564		I2S_50S	I2S	I2S0 CODEC ASP_SDOUT		15
565		I2S_50S	I2S	NC_I2S1_MCK		5
566		I2S_50S	I2S	I2S1 CODEC_XSP_BCLK		5 15
567		I2S_50S	I2S	I2S1 CODEC_XSP_LRCK		5 15
568		I2S_50S	I2S	I2S1 CODEC_XSP_DIN		5 15
569		I2S_50S	I2S	I2S1 CODEC_XSP_DOUT		5 15
570		I2S_50S	I2S	I2S1 CODEC_XSP_SDOUT		15
571		I2S_50S	CLK	NC_I2S2_MCK_R		5
572		I2S_50S	CLK	NC_I2S2_MCK		5
573		I2S_50S	I2S	NC_I2S2_BCLK		5
574		I2S_50S	I2S	NC_I2S2_LRCK		5
575		I2S_50S	I2S	NC_I2S2_DIN		5
576		I2S_50S	I2S	NC_I2S2_DOUT		5
577		I2S_50S	I2S	NC_I2S4_MCK		5
578		I2S_50S	I2S	I2S4_SOC2BT_BCLK		5 46
579		I2S_50S	I2S	I2S4_SOC2BT_LRCK		5 46
580		I2S_50S	I2S	I2S4_SOC2BT_DATA		5 46
581		I2S_50S	I2S	I2S4_BT2SOC_DATA		5 46

DWI

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DWI	*	*	2:1_SPACING

ELECTRICAL_CONSTRAINT_SET		NET_TYPE		PHYSICAL	SPACING	
582			DWI	DWI AP_CLK		5 57
583			DWI	NC_DWI_AP_DI		57
584			DWI	DWI_AP_DO		5 57

I2C

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
I2C_50S	*	45_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
I2C	*	*	1.5:1_SPACING

ELECTRICAL_CONSTRAINT_SET		NET_TYPE		PHYSICAL	SPACING	
585		I2C_50S	I2C	I2C0_SDA_Iv8		5 57 60
586		I2C_50S	I2C	I2C0_SCL_Iv8		5 57 60
587		I2C_50S	I2C	I2C3_CAM_ALS_SDA_Iv8_F		22 60
588		I2C_50S	I2C	I2C3_CAM_ALS_SCL_Iv8_F		22 60
589		I2C_50S	I2C	I2C0_HP_ALS_SDA_Iv8_FILT		60
590		I2C_50S	I2C	I2C0_HP_ALS_SCL_Iv8_FILT		60
591		I2C_50S	I2C	I2C1_SOC2OSCAR_SWDCCLK_Iv8		5 19
592		I2C_50S	I2C	I2C1_SOC2OSCAR_SWDIO_Iv8		5 19
593		I2C_50S	I2C	I2C2_SDA_Iv8		5 47
594		I2C_50S	I2C	I2C2_SCL_Iv8		5 47
595		I2C_50S	I2C	I2C3_SDA_Iv8		5 13 22 61
596		I2C_50S	I2C	I2C3_SCL_Iv8		5 13 22 61
597		I2C_50S	I2C	DMIC1_FF_SD_FILT		16 60
598		I2C_50S	I2C	DMIC1_FF_SCLK_FILT		16 60
599		I2C_50S	I2C	DMIC1_FF_SD		15 16
600		I2C_50S	I2C	DMIC1_FF_SCLK		15 16
601		I2C_50S	I2C	SEP_I2C0_SCL		5
602		I2C_50S	I2C	SEP_I2C0_SDA		5
603		I2C_50S	I2C	ISP0_CAM_REAR_SCL		7 23
604		I2C_50S	I2C	ISP0_CAM_REAR_SDA		7 23
605		I2C_50S	I2C	ISP0_CAM_REAR_SCL_F		23 60
606		I2C_50S	I2C	ISP0_CAM_REAR_SDA_F		23 60
607		I2C_50S	I2C	ISP1_CAM_FRONT_SCL		7 22
608		I2C_50S	I2C	ISP1_CAM_FRONT_SDA		7 22
609		I2C_50S	I2C	ISP1_CAM_FRONT_SCL_F		22 60
610		I2C_50S	I2C	ISP1_CAM_FRONT_SDA_F		22 60

SPI

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
SPI_50S	*	45_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SPI	*	*	2:1_SPACING

ELECTRICAL_CONSTRAINT_SET		NET_TYPE		PHYSICAL	SPACING	
611		SPI_50S	SPT	SPI3_CODEC_MISO		5 15
612		SPI_50S	SPT	SPI3_CODEC_MOSI		5 15
613		SPI_50S	SPT	SPI3_CODEC_SCLK		5 15
614		SPI_50S	SPT	SPI3_CODEC_CS_L		5 15
615		SPI_50S	SPT	SPI2_GRAPE_MISO		5 52 60 61 64
616		SPI_50S	SPT	SPI2_GRAPE_MOSI		5 52 60 61 64
617		SPI_50S	SPT	SPI2_GRAPE_SCLK		5 52 60 61 64
618		SPI_50S	SPT	SPI2_GRAPE_CS_L		5 52 60 61 64
619		SPI_50S	SPT	SPI2_GRAPE_MISO		5 52 60 61 64
620		SPI_50S	SPT	SPI2_GRAPE_MOSI		5 52 60 61 64
621		SPI_50S	SPT	SPI2_GRAPE_SCLK		5 52 60 61 64
622		SPI_50S	SPT	SPI2_GRAPE_CS_L		5 52 60 61 64
623		SPI_50S	SPT	SPI_OSCAR_MISO		19 24
624		SPI_50S	SPT	SPI_OSCAR_MOSI		19 24
625		SPI_50S	SPT	SPI_OSCAR_SCLK		19 24
626		SPI_50S	SPT	SPI_OSCAR_MISO_GYRO		19
627		SPI_50S	SPT	SPI_OSCAR_MISO_ACCEL		19
628		SPI_50S	SPT	SPI_OSCAR_MISO_COMP1		24
629		SPI_50S	SPT	SPI_OSCAR_MOSI_R		19
630		SPI_50S	SPT	SPI_OSCAR_SCLK_R		19
631		SPI_50S	SPT	SPI_OSCAR2ACCEL_CS_L		19
632		SPI_50S	SPT	SPI_OSCAR2GYRO_CS_L		19
633		SPI_50S	SPT	SPI_OSCAR2COMPASS_CS_L		19 24

JTAG

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
JTAG	*	*	2:1_SPACING

ELECTRICAL_CONSTRAINT_SET		NET_TYPE		PHYSICAL	SPACING	
634			JTAG	JTAG_SOC_TCK		4 47 60
635			JTAG	JTAG_SOC_TMS		4 47 60
636			JTAG	JTAG_SOC_TDI		4 60
637			JTAG	TP_JTAG_SOC_TDO		4 60
638			RST	JTAG_SOC_TRST_L		4 13 60
639			JTAG	NC_JTAG_SOC_TRTCK		4
640			JTAG	BB_JTAG_TMS		5 25 28 61
641			JTAG	BB_JTAG_TCK		5 25 28 61
642			JTAG	BB_JTAG_TDO		5 25 28 61
643			JTAG	BB_JTAG_TDI		5 25 28 61
644			RST	BB_JTAG_TRST_L		5 25 28 61
645			JTAG	JTAG_WLAN_TMS_TX_BLANK		46 61
646			JTAG	TP_JTAG_WLAN_TCK		46 61
647			JTAG	JTAG_WLAN_TDO_OSCAR_B		46 61
648			JTAG	JTAG_WLAN_TDI_OSCAR_A		46 61
649			RST	TP_JTAG_WLAN_TRST_L		46 61
650			JTAG	TP_JTAG_CUMULUS_M_TCK		52 61
651			JTAG	TP_JTAG_CUMULUS_M_TDI		52 61
652			JTAG	JTAG_CUMULUS_M_TMS		52 61
653			JTAG	TP_JTAG_CUMULUS_M_TDO		52 61

USB

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET	NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
USB_90D	*	90_OHM_DIFF	USB	*	*	4:1_SPACING

ELECTRICAL_CONSTRAINT_SET		NET_TYPE		PHYSICAL	SPACING	
654		USB	USB_90D	USB	USB_SOC_P	4 47 60
655		USB	USB_90D	USB	USB_SOC_N	4 47 60
656		USB	USB_90D	USB	USB_BB_P	25 47
657		USB	USB_90D	USB	USB_BB_N	25 47
658		USB	USB_90D	USB	USB_BB_DEBUG_P	25 28 61
659		USB	USB_90D	USB	USB_BB_DEBUG_N	25 28 61
660		USB	USB_90D	USB	E75_DPAIR1_CONN_P	47 49 60
661		USB	USB_90D	USB	E75_DPAIR1_CONN_N	47 49 60
662		USB	USB_90D	USB	E75_DPAIR2_CONN_P	47 49 60
663		USB	USB_90D	USB	E75_DPAIR2_CONN_N	47 49 60
664		USB	USB_90D	USB	E75_DPAIR1_P	47
665		USB	USB_90D	USB	E75_DPAIR1_N	47
666		USB	USB_90D	USB	E75_DPAIR2_P	47
667		USB	USB_90D	USB	E75_DPAIR2_N	47

HSIC

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
HSIC	*	45_OHM_SE

ELECTRICAL_CONSTRAINT_SET		NET_TYPE		PHYSICAL	SPACING	
668		HSIC	HSIC		HSIC1_WLAN_DATA	4 46 61
669		HSIC	HSIC		HSIC1_WLAN_STB	4 46 61
670		HSIC	HSIC		HSIC2_BB_DATA	4 25 28 61
671		HSIC	HSIC		HSIC2_BB_STB	4 25 28 61
672		HSIC	HSIC		NC_HSIC0_DATA	4
673		HSIC	HSIC		NC_HSIC0_STB	4
674		HSIC	HSIC_RDY		HSIC1_WLAN2SOC_REMOTE_WAKE	5 46 61
675		HSIC	HSIC_RDY		HSIC1_WLAN2SOC_DEVICE_RDY	5 46 61
676		HSIC	HSIC_RDY		HSIC1_SOC2WLAN_HOST_RDY	5 46 61
677		HSIC	HSIC_RDY		HSIC1_SOC2WLAN_HOST_RDY_R	46 61
678		HSIC	HSIC_RDY		HSIC2_BB2SOC_REMOTE_WAKE	5 29
679		HSIC	HSIC_RDY		HSIC2_BB2SOC_DEVICE_RDY	5 25 29
680		HSIC	HSIC_RDY		HSIC2_SOC2BB_HOST_RDY	5 25 29

MIPI

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET	MIPI0C	*	*	4:1_SPACING
MIPI_90D	*	90_OHM_DIFF	MIPI1C	*	*	4:1_SPACING

ELECTRICAL CONSTRAINT SET		NET_TYPE		
		PHYSICAL	SPACING	
MIPI0C_PP	MIPI0C_PP	MIPT_90D	MIPT0C	MIPI0C_CAM_REAR_CLK_P 7 23 61
MIPI0C_PP	MIPI0C_PP	MIPT_90D	MIPT0C	MIPI0C_CAM_REAR_CLK_N 7 23 61
MIPI0C_PP	MIPI0C_PP	MIPT_90D	MIPT0C	MIPI0C_CAM_REAR_DATA_P<0> 7 23 61
MIPI0C_PP	MIPI0C_PP	MIPT_90D	MIPT0C	MIPI0C_CAM_REAR_DATA_N<0> 7 23 61
MIPI0C_PP	MIPI0C_PP	MIPT_90D	MIPT0C	MIPI0C_CAM_REAR_DATA_P<1> 7 23 61
MIPI0C_PP	MIPI0C_PP	MIPT_90D	MIPT0C	MIPI0C_CAM_REAR_DATA_N<1> 7 23 61
MIPI0C_PP	MIPI0C_PP	MIPT_90D	MIPT0C	NC_MIPI0C_CAM_REAR_DATA_P<2> 7
MIPI0C_PP	MIPI0C_PP	MIPT_90D	MIPT0C	NC_MIPI0C_CAM_REAR_DATA_N<2> 7
MIPI0C_PP	MIPI0C_PP	MIPT_90D	MIPT0C	NC_MIPI0C_CAM_REAR_DATA_P<3> 7
MIPI0C_PP	MIPI0C_PP	MIPT_90D	MIPT0C	NC_MIPI0C_CAM_REAR_DATA_N<3> 7
MIPI0C_PP	MIPI0C_PP	MIPT_90D	MIPT0C	MIPI0C_CAM_REAR_CLK_FILT_P 23 61
MIPI0C_PP	MIPI0C_PP	MIPT_90D	MIPT0C	MIPI0C_CAM_REAR_CLK_FILT_N 23 61
MIPI0C_PP	MIPI0C_PP	MIPT_90D	MIPT0C	MIPI0C_CAM_REAR_DATA_FILT_P<0> 23 61
MIPI0C_PP	MIPI0C_PP	MIPT_90D	MIPT0C	MIPI0C_CAM_REAR_DATA_FILT_N<0> 23 61
MIPI0C_PP	MIPI0C_PP	MIPT_90D	MIPT0C	MIPI0C_CAM_REAR_DATA_FILT_P<1> 23 61
MIPI0C_PP	MIPI0C_PP	MIPT_90D	MIPT0C	MIPI0C_CAM_REAR_DATA_FILT_N<1> 23 61
MIPI0C_PP	MIPI0C_PP	MIPT_90D	MIPT0C	NC_MIPI0C_CAM_REAR_DATA_FILT_P<2> 23 61
MIPI0C_PP	MIPI0C_PP	MIPT_90D	MIPT0C	NC_MIPI0C_CAM_REAR_DATA_FILT_N<2> 23 61
MIPI0C_PP	MIPI0C_PP	MIPT_90D	MIPT0C	NC_MIPI0C_CAM_REAR_DATA_FILT_P<3> 23 61
MIPI0C_PP	MIPI0C_PP	MIPT_90D	MIPT0C	NC_MIPI0C_CAM_REAR_DATA_FILT_N<3> 23 61
MIPI1C_PP	MIPI1C_PP	MIPT_90D	MIPT1C	MIPI1C_CAM_FRONT_CLK_P 7 22 61
MIPI1C_PP	MIPI1C_PP	MIPT_90D	MIPT1C	MIPI1C_CAM_FRONT_CLK_N 7 22 61
MIPI1C_PP	MIPI1C_PP	MIPT_90D	MIPT1C	MIPI1C_CAM_FRONT_DATA_P<0> 7 22 61
MIPI1C_PP	MIPI1C_PP	MIPT_90D	MIPT1C	MIPI1C_CAM_FRONT_DATA_N<0> 7 22 61
MIPI1C_PP	MIPI1C_PP	MIPT_90D	MIPT1C	NC_MIPI1C_CAM_FRONT_DATA_P<1> 7
MIPI1C_PP	MIPI1C_PP	MIPT_90D	MIPT1C	NC_MIPI1C_CAM_FRONT_DATA_N<1> 7
MIPI1C_PP	MIPI1C_PP	MIPT_90D	MIPT1C	MIPI1C_CAM_FRONT_CLK_FILT_P 22 61
MIPI1C_PP	MIPI1C_PP	MIPT_90D	MIPT1C	MIPI1C_CAM_FRONT_CLK_FILT_N 22 61
MIPI1C_PP	MIPI1C_PP	MIPT_90D	MIPT1C	MIPI1C_CAM_FRONT_DATA_FILT_P<0> 22 61
MIPI1C_PP	MIPI1C_PP	MIPT_90D	MIPT1C	MIPI1C_CAM_FRONT_DATA_FILT_N<0> 22 61
MIPI1D_PP	MIPI1D_PP	MIPT_90D	MIPT1C	NC_MIPI1D_DPCLK 7
MIPI1D_PP	MIPI1D_PP	MIPT_90D	MIPT1C	NC_MIPI1D_DNCLK 7
MIPI1D_PP	MIPI1D_PP	MIPT_90D	MIPT1C	NC_MIPI1D_DPDATA0 7
MIPI1D_PP	MIPI1D_PP	MIPT_90D	MIPT1C	NC_MIPI1D_DNDATA0 7
MIPI1D_PP	MIPI1D_PP	MIPT_90D	MIPT1C	NC_MIPI1D_DPDATA1 7
MIPI1D_PP	MIPI1D_PP	MIPT_90D	MIPT1C	NC_MIPI1D_DNDATA1 7
MIPI1D_PP	MIPI1D_PP	MIPT_90D	MIPT1C	NC_MIPI1D_DPDATA2 7
MIPI1D_PP	MIPI1D_PP	MIPT_90D	MIPT1C	NC_MIPI1D_DNDATA2 7
MIPI1D_PP	MIPI1D_PP	MIPT_90D	MIPT1C	NC_MIPI1D_DPDATA3 7
MIPI1D_PP	MIPI1D_PP	MIPT_90D	MIPT1C	NC_MIPI1D_DNDATA3 7
MIPI2C_PP	MIPI2C_PP	MIPT_90D	MIPT0C	MIPI2CAM0_CLKCON_P
MIPI2C_PP	MIPI2C_PP	MIPT_90D	MIPT0C	MIPI2CAM0_CLKCON_N
MIPI2C_PP	MIPI2C_PP	MIPT_90D	MIPT0C	MIPI2CAM0_DOCON_P
MIPI2C_PP	MIPI2C_PP	MIPT_90D	MIPT0C	MIPI2CAM0_DOCON_N
MIPI2C_PP	MIPI2C_PP	MIPT_90D	MIPT0C	MIPI2CAM0_DICON_P
MIPI2C_PP	MIPI2C_PP	MIPT_90D	MIPT0C	MIPI2CAM0_DICON_N
MIPI2C_PP	MIPI2C_PP	MIPT_90D	MIPT0C	MIPI2CAM0_D2CON_P
MIPI2C_PP	MIPI2C_PP	MIPT_90D	MIPT0C	MIPI2CAM0_D2CON_N
MIPI2C_PP	MIPI2C_PP	MIPT_90D	MIPT0C	MIPI2CAM0_D3CON_P
MIPI2C_PP	MIPI2C_PP	MIPT_90D	MIPT0C	MIPI2CAM0_D3CON_N
MIPI2C_PP	MIPI2C_PP	MIPT_90D	MIPT1C	MIPI2CAM1_CLKCON_P
MIPI2C_PP	MIPI2C_PP	MIPT_90D	MIPT1C	MIPI2CAM1_CLKCON_N
MIPI2C_PP	MIPI2C_PP	MIPT_90D	MIPT1C	MIPI2CAM1_DOCON_P
MIPI2C_PP	MIPI2C_PP	MIPT_90D	MIPT1C	MIPI2CAM1_DOCON_N
MIPI2C_PP	MIPI2C_PP	MIPT_90D	MIPT1C	MIPI2CAM1_DICON_P
MIPI2C_PP	MIPI2C_PP	MIPT_90D	MIPT1C	MIPI2CAM1_DICON_N

BACKLIGHT

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET	NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
LED	*	LED	LEDA	*	*	2.4:1_SPACING
			LEDB	*	*	2.4:1_SPACING

ELECTRICAL_CONSTRAINT_SET		NET_TYPE		
		PHYSICAL	SPACING	
LED1	LED	LED A	LED IO1 A R	56
LED2	LED	LED B	LED IO1 B R	56
LED3	LED	LED A	LED IO2 A R	56
LED4	LED	LED B	LED IO2 B R	56
LED5	LED	LED A	LED IO3 A R	56
LED6	LED	LED B	LED IO3 B R	56
LED7	LED	LED A	LED IO4 A R	56
LED8	LED	LED B	LED IO4 B R	56
LED9	LED	LED A	LED IO5 A R	56
LED10	LED	LED B	LED IO5 B R	56
LED11	LED	LED A	LED IO6 A R	56
LED12	LED	LED B	LED IO6 B R	56
LED13	LED	LED A	LED IO 1 A	53 56 60
LED14	LED	LED B	LED IO 1 B	53 56 60
LED15	LED	LED A	LED IO 2 A	53 56 60
LED16	LED	LED B	LED IO 2 B	53 56 60
LED17	LED	LED A	LED IO 3 A	53 56 60
LED18	LED	LED B	LED IO 3 B	53 56 60
LED19	LED	LED A	LED IO 4 A	53 56 60
LED20	LED	LED B	LED IO 4 B	53 56 60
LED21	LED	LED A	LED IO 5 A	53 56 60
LED22	LED	LED B	LED IO 5 B	53 56 60
LED23	LED	LED A	LED IO 6 A	53 56 60
LED24	LED	LED B	LED IO 6 B	53 56 60

AUDIO/SPEAKER

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
AUDIO	*	*	3:1_SPACING
AUDIO	AUDIO	*	2:1_SPACING

ELECTRICAL_CONSTRAINT_SET		NET_TYPE		
		PHYSICAL	SPACING	
SPKR_DIFF	SPEAKER	AUDIO	SPKRAMP L1 OUT P	18 49 60
SPKR_DIFF	SPEAKER	AUDIO	SPKRAMP L1 OUT N	18 49 60
SPKR_DIFF	SPEAKER	AUDIO	SPKRAMP L2 OUT P	18 49 60
SPKR_DIFF	SPEAKER	AUDIO	SPKRAMP L2 OUT N	18 49 60
SPKR_DIFF	SPEAKER	AUDIO	SPKRAMP R1 OUT P	17 49 60
SPKR_DIFF	SPEAKER	AUDIO	SPKRAMP R1 OUT N	17 49 60
SPKR_DIFF	SPEAKER	AUDIO	SPKRAMP R2 OUT P	17 49 60
SPKR_DIFF	SPEAKER	AUDIO	SPKRAMP R2 OUT N	17 49 60
	USB_90D	USB	MIKEY TS P	15 47
	USB_90D	USB	MIKEY TS N	15 47
	MAXIMUM NECK LENGTH=0.5 MM MIN NECK WIDTH=0.06 MM	USB	L81 MBUS P	15 47
	USB_90D	USB	L81 MBUS N	15
SPKR_DIFF	AUDIO_DIFF	AUDIO	LEFT CH OUT P	15 18 60
SPKR_DIFF	AUDIO_DIFF	AUDIO	LEFT CH OUT N	15 18 60
SPKR_DIFF	AUDIO_DIFF	AUDIO	RIGHT CH OUT P	15 18 60
SPKR_DIFF	AUDIO_DIFF	AUDIO	RIGHT CH OUT N	15 18 60
SPKR_DIFF	AUDIO_DIFF	AUDIO	MAX98304 L1 IN P	18 61
SPKR_DIFF	AUDIO_DIFF	AUDIO	MAX98304 L1 IN N	18 61
SPKR_DIFF	AUDIO_DIFF	AUDIO	MAX98304 R1 IN P	17 61
SPKR_DIFF	AUDIO_DIFF	AUDIO	MAX98304 R1 IN N	17 61
SPKR_DIFF	AUDIO_DIFF	AUDIO	MAX98304 L2 IN P	18 61
SPKR_DIFF	AUDIO_DIFF	AUDIO	MAX98304 L2 IN N	18 61
SPKR_DIFF	AUDIO_DIFF	AUDIO	MAX98304 R2 IN P	17 61
SPKR_DIFF	AUDIO_DIFF	AUDIO	MAX98304 R2 IN N	17 61
	AUDIO_DIFF	AUDIO	SPKR L1 VSNS P	
	AUDIO_DIFF	AUDIO	SPKR L1 VSNS N	
	AUDIO_DIFF	AUDIO	SPKR R1 VSNS P	
	AUDIO_DIFF	AUDIO	SPKR R1 VSNS N	
	MAXIMUM NECK LENGTH=15 MM	AUDIO	CODEC HP HS3	15
	PWR_0P5MM	AUDIO	CODEC HP HS4	15
	PWR_0P5MM	AUDIO	CONN HP HS3 FILT	15 16 60
	PWR_0P5MM	AUDIO	CONN HP HS4 FILT	15 16 60
	PWR_0P2MM	AUDIO	CODEC HP LEFT	15
	PWR_0P2MM	AUDIO	CODEC HP RIGHT	15
	PWR_0P2MM	AUDIO	CONN HP LEFT FILT	15 16 60
	PWR_0P2MM	AUDIO	CONN HP RIGHT FILT	15 16 60
	PP_PWR	PWR	L81 NVCP	15 61
	PP_PWR	PWR	L81 PVCP	15 61
	PP_PWR	PWR	L81 FLYP	15 61
	PP_PWR	PWR	L81 FLYN	15 61
	PP_PWR	PWR	L81 FLCV	15 61
	PP_PWR	PWR	SPEAKER VO	
	PP_PWR	PWR	L81 FILT	15
	PWR_0P1MM	AUDIO	HP MIC POS	15
	PWR_0P1MM	AUDIO	HP MIC NEG	15
	PWR_0P1MM	AUDIO	L81 AIN2 POS	15
	PWR_0P1MM	AUDIO	L81 AIN2 NEG	15
	PWR_0P1MM	AUDIO	CODEC HP HS3_REF	15
	PWR_0P1MM	AUDIO	CODEC HP HS4_REF	15
	PWR_0P1MM	AUDIO	CONN HP HS3_REF FILT	15 16 60
	PWR_0P1MM	AUDIO	CONN HP HS4_REF FILT	15 16 60

XTAL

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CRYSTAL	*	*	5:1_SPACING

ELECTRICAL_CONSTRAINT_SET	SET_TYPE		
	PHYSICAL	SPACING	
CRISTAL		CRYSTAL	XTAL_SOC 24M I 4
CRISTAL		CRYSTAL	XTAL_SOC 24M O 4
CRISTAL		CRYSTAL	SOC 24M O 4
CRISTAL		CRYSTAL	PMU XTAL 56
CRISTAL		CRYSTAL	PMU EXTAL 56

EMBEDDED DISPLAYPORT

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET	NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
EDP_90D	*	90_OHM_DIFF	EDP_50S	*	45_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
EDP	*	*	4:1_SPACING

ELECTRICAL_CONSTRAINT_SET		NET_TYPE	SPACING	
		EDP_90D	EDP	EDP AUX P
		EDP_90D	EDP	EDP AUX N
		EDP_50S	EDP	EDP HPD
	EDP	EDP_90D	EDP	EDP DATA P<0>
	EDP	EDP_90D	EDP	EDP DATA N<0>
	EDP	EDP_90D	EDP	EDP DATA P<1>
	EDP	EDP_90D	EDP	EDP DATA N<1>
	EDP	EDP_90D	EDP	EDP DATA P<2>
	EDP	EDP_90D	EDP	EDP DATA N<2>
	EDP	EDP_90D	EDP	EDP DATA P<3>
	EDP	EDP_90D	EDP	EDP DATA N<3>
		EDP_90D	EDP	EDP AUX EMI P
		EDP_90D	EDP	EDP AUX EMI N
	EDP	EDP_90D	EDP	EDP DATA EMI P<0>
	EDP	EDP_90D	EDP	EDP DATA EMI N<0>
	EDP	EDP_90D	EDP	EDP DATA EMI P<1>
	EDP	EDP_90D	EDP	EDP DATA EMI N<1>
	EDP	EDP_90D	EDP	EDP DATA EMI P<2>
	EDP	EDP_90D	EDP	EDP DATA EMI N<2>
	EDP	EDP_90D	EDP	EDP DATA EMI P<3>
	EDP	EDP_90D	EDP	EDP DATA EMI N<3>
		EDP_90D	EDP	EDP AUX EMI CONN P
		EDP_90D	EDP	EDP AUX EMI CONN N
	EDP	EDP_90D	EDP	EDP DATA EMI CONN P<0>
	EDP	EDP_90D	EDP	EDP DATA EMI CONN N<0>
	EDP	EDP_90D	EDP	EDP DATA EMI CONN P<1>
	EDP	EDP_90D	EDP	EDP DATA EMI CONN N<1>
	EDP	EDP_90D	EDP	EDP DATA EMI CONN P<2>
	EDP	EDP_90D	EDP	EDP DATA EMI CONN N<2>
	EDP	EDP_90D	EDP	EDP DATA EMI CONN P<3>
	EDP	EDP_90D	EDP	EDP DATA EMI CONN N<3>

TEMP SENSORS

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET	NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
BOARD_TEMP	*	TEMP_SENSE	BOARD_TEMP	*	*	3:1_SPACING

ELECTRICAL_CONSTRAINT_SET		NET_TYPE						
		PHYSICAL	SPACING					
MIN	BOARD_TEMP	NECK_WIDTH=0.053	BOARD_TEMP	MIN	BOARD_TEMP	PA_NTC_P	57	60
MAX	BOARD_TEMP	NECK_WIDTH=0.053	BOARD_TEMP	MAX	BOARD_TEMP	PA_NTC_N	57	
MIN	BOARD_TEMP		BOARD_TEMP		BOARD_TEMP	BOARD_TEMP2_P	57	60
MAX	BOARD_TEMP		BOARD_TEMP		BOARD_TEMP	BOARD_TEMP2_N	57	
MIN	BOARD_TEMP		BOARD_TEMP		BOARD_TEMP	BOARD_TEMP3_P	57	60
MAX	BOARD_TEMP		BOARD_TEMP		BOARD_TEMP	BOARD_TEMP3_N	57	
MIN	BOARD_TEMP		BOARD_TEMP		BOARD_TEMP	BOARD_TEMP4_P	57	60
MAX	BOARD_TEMP		BOARD_TEMP		BOARD_TEMP	BOARD_TEMP4_N	57	
MIN	BOARD_TEMP		BOARD_TEMP		BOARD_TEMP	BOARD_TEMP5_P	57	60
MAX	BOARD_TEMP		BOARD_TEMP		BOARD_TEMP	BOARD_TEMP5_N	57	
MIN	BOARD_TEMP		BOARD_TEMP		BOARD_TEMP	BOARD_TEMP6_P	57	60
MAX	BOARD_TEMP		BOARD_TEMP		BOARD_TEMP	BOARD_TEMP6_N	57	
MIN	BOARD_TEMP		BOARD_TEMP		BOARD_TEMP	BOARD_TEMP7_P	57	60
MAX	BOARD_TEMP		BOARD_TEMP		BOARD_TEMP	BOARD_TEMP7_N	57	
MIN	BOARD_TEMP		BOARD_TEMP		BOARD_TEMP	BOARD_TEMP8_P	57	60
MAX	BOARD_TEMP		BOARD_TEMP		BOARD_TEMP	BOARD_TEMP8_N	57	

GRAPE

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
GRAPE	*	GRAPE_SE

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
MT2	GRAPE	GRAPE	MT_PANEL_IN<0..29>	52 61
MT4	GRAPE	GRAPE	MT_PANEL_OUT<0..39>	52 61



DDR						
NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET	NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DDR_50S	*	DRAM_SE	DDR	*	*	3:1_SPACING

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
DDR_90D	*	DRAM_DIFF

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
8322	DDR_50S	DDR	DDR0_CA<0>	8 12 61
8323	DDR_50S	DDR	DDR0_CA<9..1>	8 12 61
8324	DDR_50S	DDR	DDR0_DM<3..0>	8 12 61
8325	DDR_90D	DDR	DDR0_CK_P	8 12 61
8326	DDR_90D	DDR	DDR0_CK_N	8 12 61
8327	DDR_50S	DDR	DDR0_CKE<1..0>	8 12 61
8328	DDR_50S	DDR	DDR0_CSN<1..0>	8 12 61
8329		DDR	DDR0_CA_ZQ_SOC	8
8330		DDR	DDR0_DQ_ZQ_SOC	8
8331		DDR	DDR0_ZQ_DRAM	12
8332	DDR_50S	DDR	DDR0_DQ<1..0>	8 12 61
8333	DDR_50S	DDR	DDR0_DQ<2>	8 12 61
8334	DDR_50S	DDR	DDR0_DQ<7..3>	8 12 61
8335	DDR_90D	DDR	DDR0_DQS_P<0>	8 12 61
8336	DDR_90D	DDR	DDR0_DQS_N<0>	8 12 61
8337	DDR_50S	DDR	DDR0_DQ<15..8>	8 12 61
8338	DDR_90D	DDR	DDR0_DQS_P<1>	8 12 61
8339	DDR_90D	DDR	DDR0_DQS_N<1>	8 12 61
8340	DDR_50S	DDR	DDR0_DQ<23..16>	8 12 61
8341	DDR_90D	DDR	DDR0_DQS_P<2>	8 12 61
8342	DDR_90D	DDR	DDR0_DQS_N<2>	8 12 61
8343	DDR_50S	DDR	DDR0_DQ<27..25>	8 12 61
8344	DDR_50S	DDR	DDR0_DQ<28>	8 12 61
8345	DDR_50S	DDR	DDR0_DQ<31..29>	8 12 61
8346	DDR_90D	DDR	DDR0_DQS_P<3>	8 12 61
8347	DDR_90D	DDR	DDR0_DQS_N<3>	8 12 61
8348				
8349	DDR_50S	DDR	DDR1_CA<3..0>	8 12 61
8350	DDR_50S	DDR	DDR1_CA<9..4>	8 12 61
8351	DDR_50S	DDR	DDR1_DM<3..0>	8 12 61
8352	DDR_90D	DDR	DDR1_CK_P	8 12 61
8353	DDR_90D	DDR	DDR1_CK_N	8 12 61
8354	DDR_50S	DDR	DDR1_CKE<1..0>	8 12 61
8355	DDR_50S	DDR	DDR1_CSN<0>	8 12 61
8356	DDR_50S	DDR	DDR1_CSN<1>	8 12 61
8357				
8358		DDR	DDR1_CA_ZQ_SOC	8
8359		DDR	DDR1_DQ_ZQ_SOC	8
8360		DDR	DDR1_ZQ_DRAM	12
8361	DDR_50S	DDR	DDR1_DQ<7..0>	8 12 61
8362	DDR_90D	DDR	DDR1_DQS_P<0>	8 12 61
8363	DDR_90D	DDR	DDR1_DQS_N<0>	8 12 61
8364	DDR_50S	DDR	DDR1_DQ<15..8>	8 12 61
8365	DDR_90D	DDR	DDR1_DQS_P<1>	8 12 61
8366	DDR_90D	DDR	DDR1_DQS_N<1>	8 12 61
8367	DDR_50S	DDR	DDR1_DQ<23..16>	8 12 61
8368	DDR_90D	DDR	DDR1_DQS_P<2>	8 12 61
8369	DDR_90D	DDR	DDR1_DQS_N<2>	8 12 61
8370	DDR_50S	DDR	DDR1_DQ<31..24>	8 12 61
8371	DDR_90D	DDR	DDR1_DQS_P<3>	8 12 61
8372	DDR_90D	DDR	DDR1_DQS_N<3>	8 12 61

VREF (DDR/FMI)			
NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
VREF	*	*	5:1_SPACING

VOLTAGE	NET_TYPE			
	PHYSICAL	SPACING		
8373	0.6V	PP_PWR	PPVREF_DDR0_CA_SOC	8
8374	0.6V	PP_PWR	PPVREF_DDR0_DQ_SOC	8
8375	0.6V	PP_PWR	PPVREF_DDR1_CA_SOC	8
8376	0.6V	PP_PWR	PPVREF_DDR1_DQ_SOC	8
8377	0.6V	PP_PWR	PPVREF_DDR0_CA_DRAM	12
8378	0.6V	PP_PWR	PPVREF_DDR0_DQ_DRAM	12
8379	0.6V	PP_PWR	PPVREF_DDR1_CA_DRAM	12
8380	0.6V	PP_PWR	PPVREF_DDR1_DQ_DRAM	12
8381				
8382	0.9V	PP_PWR	PPVREF_FMI_SOC	6 61
8383	0.9V	PP_PWR	PPVREF_FMI_NAND	14 61

NAND				
NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET		
NAND_50S	*	45_OHM_SE		

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
NAND	*	*	3:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
8384	FMI0_AD_CTRL_PP	NAND_50S	FMI0_AD<0>	6 14 61
8385	FMI0_AD_CTRL	NAND_50S	FMI0_AD<1>	6 14 61
8386	FMI0_AD_CTRL	NAND_50S	FMI0_AD<2>	6 14 61
8387	FMI0_AD_CTRL	NAND_50S	FMI0_AD<3>	6 14 61
8388	FMI0_AD_CTRL	NAND_50S	FMI0_AD<4>	6 14 61
8389	FMI0_AD_CTRL	NAND_50S	FMI0_AD<5>	6 14 61
8390	FMI0_AD_CTRL	NAND_50S	FMI0_AD<6>	6 14 61
8391	FMI0_AD_CTRL	NAND_50S	FMI0_AD<7>	6 14 61
8392	FMI0_AD_CTRL	NAND_50S	FMI0_ALE	6 14 61
8393	FMI0_CE	NAND_50S	FMI0_CE0_L	6 14 60 61
8394	FMI0_AD_CTRL	NAND_50S	FMI0_CLE	6 14 61
8395		NAND_50S	FMI0_DQS	6 14 61
8396	FMI0_AD_CTRL	NAND_50S	FMI0_RE_L	6 14 61
8397	FMI0_AD_CTRL	NAND_50S	FMI0_WE_L	6 14 61
8398				
8399	FMI1_AD_CTRL	NAND_50S	FMI1_AD<0>	6 14 61
8400	FMI1_AD_CTRL	NAND_50S	FMI1_AD<1>	6 14
8401	FMI1_AD_CTRL	NAND_50S	FMI1_AD<2>	6 14
8402	FMI1_AD_CTRL	NAND_50S	FMI1_AD<3>	6 14
8403	FMI1_AD_CTRL	NAND_50S	FMI1_AD<4>	6 14
8404	FMI1_AD_CTRL	NAND_50S	FMI1_AD<5>	6 14
8405	FMI1_AD_CTRL	NAND_50S	FMI1_AD<6>	6 14
8406	FMI1_AD_CTRL	NAND_50S	FMI1_AD<7>	6 14
8407	FMI1_AD_CTRL	NAND_50S	FMI1_ALE	6 14 61
8408	FMI1_CE	NAND_50S	FMI1_CE0_L	6 14 61
8409	FMI1_AD_CTRL	NAND_50S	FMI1_CLE	6 14 61
8410	FMI1_AD_CTRL	NAND_50S	FMI1_DQS	6 14 61
8411	FMI1_AD_CTRL	NAND_50S	FMI1_RE_L	6 14 61
8412	FMI1_AD_CTRL	NAND_50S	FMI1_WE_L	6 14 61

NAND DEV			
ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	
8413	NAND_50S	NAND	FMI0_AD_BUF<0>
8414	NAND_50S	NAND	FMI0_AD_BUF<1>
8415	NAND_50S	NAND	FMI0_AD_BUF<2>
8416	NAND_50S	NAND	FMI0_AD_BUF<3>
8417	NAND_50S	NAND	FMI0_AD_BUF<4>
8418	NAND_50S	NAND	FMI0_AD_BUF<5>
8419	NAND_50S	NAND	FMI0_AD_BUF<6>
8420	NAND_50S	NAND	FMI0_AD_BUF<7>
8421	NAND_50S	NAND	FMI0_ALE_BUF
8422	NAND_50S	NAND	FMI0_CE0_BUF_L
8423	NAND_50S	NAND	FMI0_CLE_BUF
8424	NAND_50S	NAND	FMI0_DQS_BUF
8425	NAND_50S	NAND	FMI0_DQSN_BUF
8426	NAND_50S	NAND	FMI0_REP_BUF
8427	NAND_50S	NAND	FMI0_RE_BUF_L
8428	NAND_50S	NAND	FMI0_WE_BUF_L
8429			
8430	NAND_50S	NAND	FMI1_AD_BUF<0>
8431	NAND_50S	NAND	FMI1_AD_BUF<1>
8432	NAND_50S	NAND	FMI1_AD_BUF<2>
8433	NAND_50S	NAND	FMI1_AD_BUF<3>
8434	NAND_50S	NAND	FMI1_AD_BUF<4>
8435	NAND_50S	NAND	FMI1_AD_BUF<5>
8436	NAND_50S	NAND	FMI1_AD_BUF<6>
8437	NAND_50S	NAND	FMI1_AD_BUF<7>
8438	NAND_50S	NAND	FMI1_ALE_BUF
8439	NAND_50S	NAND	FMI1_CE0_BUF_L
8440	NAND_50S	NAND	FMI1_CLE_BUF
8441	NAND_50S	NAND	FMI1_DQS_BUF
8442	NAND_50S	NAND	FMI1_DQSN_BUF
8443	NAND_50S	NAND	FMI1_REP_BUF
8444	NAND_50S	NAND	FMI1_RE_BUF_L
8445	NAND_50S	NAND	FMI1_WE_BUF_L

RF						
NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET	NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
RF_50S	*	50_OHM_RF	100_RF	*	*	100_RF_CLEAR_SPACING
			50_RF	*	*	50_RF_SPACING
NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET	50_RF_CLEAR	*	*	50_RF_CLEAR_SPACING
RF_100D	*	100_OHM_RF	RF_60	*	*	1.2:1_SPACING

VOLTAGE		NET_TYPE		
		PHYSICAL	SPACING	
4.7V	MAX_LINE_WIDTH=1 MM PWR_RP	PWR_RP	PP BATT VCC 2G FEM	40
3.8V	MAX_LINE_WIDTH=1 MM PWR_RP	PWR_RP	PP PA	34 35 36 37 38 39 40
1.8V	MIN NECK_WIDTH=0.06 MM MAX_LINE_WIDTH=1 MM PWR_0P1MM	PWR_RP	PP LVS1	26 28
1.3V	MAX_LINE_WIDTH=1 MM PWR_RP	PWR_RP	PP RF1 1V3 DRX FE	31
4.7V UNDEFINED	MAX_LINE_WIDTH=1 MM PWR_RP	PWR_RP	PP VREG	
2.05V	MAX_LINE_WIDTH=1 MM PWR_RP	PWR_RP	PP RF2 2V05 DRX_BB	31
4.7V	MAX_LINE_WIDTH=1 MM PWR_RP	PWR_RP	PP BATT VCC PA DCDC	
1.8V	MIN NECK_WIDTH=0.06 MM MAX_LINE_WIDTH=1 MM PWR_0P1MM	PWR_RP	PP LDO1	26 60
1.8V	MAX_LINE_WIDTH=1 MM PWR_RP	PWR_RP	PP LDO2 XO HS 1V8	26 28
1.8V	MAX_LINE_WIDTH=1 MM PWR_0P1MM	PWR_RP	PP LDO3 AMUX 1V8	26 27 28
3.3V	MAX_LINE_WIDTH=1 MM PWR_0P1MM	PWR_RP	PP LDO4 VDDA 3V3	26 28
2.5V	MIN NECK_WIDTH=0.06 MM MAX_LINE_WIDTH=1 MM PWR_0P1MM	PWR_RP	PP LDO5 GPS LNA 2V5	26 42
1.8V	MAXIMUM NECK_LENGTH=5 MM MIN NECK_WIDTH=0.15 MM MAX_LINE_WIDTH=1 MM PWR_0P1MM	PWR_RP	PP LDO6 RUIIM 1V8	26 28 44 60
1.8V	MIN NECK_WIDTH=0.15 MM MAX_LINE_WIDTH=1 MM PWR_0P1MM	PWR_RP	PP LDO6 RUIIM 1V8 FILT	44
1.8V	MAX_LINE_WIDTH=1 MM PWR_0P1MM	PWR_RP	PP LDO7 DAC 1V8	26 28
1.2V	MAXIMUM NECK_LENGTH=9 MM MAX_LINE_WIDTH=1 MM PWR_0P1MM	PWR_RP	PP LDO8 VDDPX 1V2	26 28
1.05V	MAX_LINE_WIDTH=1 MM PWR_0P1MM	PWR_RP	PP LDO9 PLL 1V05	26 28
1.05V	MAX_LINE_WIDTH=1 MM PWR_0P1MM	PWR_RP	PP LDO10 ADSP 1V05	26 28
1.05V	MAX_LINE_WIDTH=1 MM PWR_0P1MM	PWR_RP	PP LDO11 MDSP FW 1V05	26 28
1.05V	MAX_LINE_WIDTH=1 MM PWR_0P1MM	PWR_RP	PP LDO12 MDSP SW 1V05	26 28
2.95V	MAX_LINE_WIDTH=1 MM PWR_0P1MM	PWR_RP	PP LDO13 VDDPX 2V95	26 28
2.65V	MAXIMUM NECK_LENGTH=4 MM MAX_LINE_WIDTH=1 MM PWR_0P1MM	PWR_RP	PP LDO14 2V65	26 33 40 41
1.05V	MAX_LINE_WIDTH=1 MM PWR_RP	PWR_RP	PP VSW S1	26
1.05V	MAX_LINE_WIDTH=1 MM PWR_0P1MM	PWR_RP	PP SMPS1 MSMC 1V05	26 60
1.3V	MAX_LINE_WIDTH=1 MM PWR_RP	PWR_RP	PP VSW S2	26
1.3V	MAX_LINE_WIDTH=1 MM PWR_RP	PWR_RP	PP SMPS2 RF1 1V3	26 31 60
1.8V	MAX_LINE_WIDTH=1 MM PWR_RP	PWR_RP	PP VSW S3	26
1.8V	MAX_LINE_WIDTH=1 MM PWR_RP	PWR_RP	PP RF1 1V8 DIG	31
1.8V	MAX_LINE_WIDTH=1 MM PWR_RP	PWR_RP	PP SMPS3 MSME 1V8 FILT	26
2.05V	MAX_LINE_WIDTH=1 MM PWR_RP	PWR_RP	PP VSW S4	26
2.05V	MAX_LINE_WIDTH=1 MM PWR_RP	PWR_RP	PP SMPS4 RF2 2V05	26 31 60
1.05V	MAX_LINE_WIDTH=1 MM PWR_RP	PWR_RP	PP VSW S5	26
1.05V	MAX_LINE_WIDTH=1 MM PWR_RP	PWR_RP	PP SMPS5 DSP 1V05	26 60
4.7V	MAX_LINE_WIDTH=1 MM PWR_RP	PWR_RP	PP BATT VCC PA DCDC_IN2	

		NET_TYPE		
		PHYSICAL	SPACING	
5001		45_OHM_SF	RF_60	50_HSIC_CAL 26
5002		RF_50S	50_RF_CLEAR	50_XCVR B13 B17 B20_TX 30 33
5003		RF_50S	50_RF	50_XCVR 2G LB_TX 30 40
5004		RF_50S	50_RF_CLEAR	50_XCVR B8_TX 30 33
5005		RF_50S	50_RF_CLEAR	50_XCVR B5 B18_TX 30 33
5006		RF_50S	50_RF_CLEAR	50_XCVR B2 B25_TX 30 32
5007		RF_50S	50_RF	50_XCVR 2G HB_TX 30 40
5008		RF_50S	50_RF_CLEAR	50_XCVR B3 B4_TX 30 32
5009		RF_50S	50_RF_CLEAR	50_XCVR B1_TX 30 32
5010		RF_50S	50_RF	50_PDET IN 30
5011		RF_50S	50_RF_CLEAR	50_PDET PAD_OUT 30
5012		RF_50S	50_RF_CLEAR	50_PDET PAD_IN 30 40
5013		RF_50S	50_RF_CLEAR	50_B1_TX SAW_IN 32 33
5014		RF_50S	50_RF_CLEAR	50_B3_B4_TX SAW_IN 32 33
5015		RF_50S	50_RF_CLEAR	50_B2_B25_TX SAW_IN 32 33
5016		RF_50S	50_RF_CLEAR	50_B1_TX SAW_OUT 33 34
5017		RF_50S	50_RF_CLEAR	50_B2_TX SAW_OUT 33 35
5018		RF_50S	50_RF_CLEAR	50_B3_TX SAW_OUT 33 35
5019		RF_50S	50_RF_CLEAR	50_B4_TX SAW_OUT 33 34
5020		RF_50S	50_RF_CLEAR	50_B5_TX SAW_OUT 33 37
5021		RF_50S	50_RF_CLEAR	50_B8_TX SAW_OUT 33 37
5022		RF_50S	50_RF_CLEAR	50_B13_TX SAW_OUT 33 38
5023		RF_50S	50_RF_CLEAR	50_B17_TX SAW_OUT 33 38
5024		RF_50S	50_RF_CLEAR	50_B20_TX SAW_OUT 33 36
5025		RF_50S	50_RF_CLEAR	50_PCS_RX
5026		RF_50S	50_RF	50_PCS_RX_MATCH
5027		RF_50S	50_RF_CLEAR	50_DCS_RX
5028		RF_50S	50_RF_CLEAR	50_DCS_RX_MATCH

		NET_TYPE		
	PHYSICAL		SPACING	
RF50S	RF 50S	50 RF CLEAR	50 B1 TX PAD IN	34
RF50S	RF 50S	50 RF CLEAR	50 B4 TX PAD IN	34
RF50S	RF 50S	50 RF CLEAR	50 B1 B4 DPLX ANT	34
RF50S	RF 50S	50 RF CLEAR	50 B1 B4 ANT	34 40
RF50S	RF 50S	50 RF CLEAR	50 B1 B4_ANT PHASESHIFT	34
RF50S	RF 50S	50 RF CLEAR	50 B2 TX PAD IN	35
RF50S	RF 50S	50 RF CLEAR	50 B3 TX PAD IN	35
RF50S	RF 50S	50 RF CLEAR	50 B2 DUPLX RX	32 35
RF50S	RF 50S	50 RF CLEAR	50 B3 DUPLX RX	32 35
RF50S	RF 50S	50 RF CLEAR	50 B2 DPLX ANT	35
RF50S	RF 50S	50 RF CLEAR	50 B3 DPLX ANT	35
RF50S	RF 50S	50 RF CLEAR	50 B2 ANT	35 40
RF50S	RF 50S	50 RF CLEAR	50 B3 ANT	35 40
RF50S	RF 50S	50 RF CLEAR	50 B2 RX BALUN	32
RF50S	RF 50S	50 RF CLEAR	50 B3 RX BALUN	32
RF50S	RF 50S	50 RF CLEAR	50 B2 ANT PHASESHIFT	35
RF50S	RF 50S	50 RF CLEAR	50 B3_ANT PHASESHIFT	35
RF50S	RF 50S	50 RF CLEAR	50 B20 TX PAD IN	36
RF50S	RF 50S	50 RF CLEAR	50 B20 DPLX ANT	36
RF50S	RF 50S	50 RF CLEAR	50 B20 ANT	36 40
RF50S	RF 50S	50 RF CLEAR	50 B20_ANT PHASESHIFT	
RF50S	RF 50S	50 RF CLEAR	50 B5 TX PAD IN	37
RF50S	RF 50S	50 RF CLEAR	50 B8 TX PAD IN	37
RF50S	RF 50S	50 RF CLEAR	50 B5 DPLX ANT	37
RF50S	RF 50S	50 RF CLEAR	50 B8 DPLX ANT	37
RF50S	RF 50S	50 RF CLEAR	50 B5 ANT	37 40
RF50S	RF 50S	50 RF CLEAR	50 B8 ANT	37 40
RF50S	RF 50S	50 RF CLEAR	50 B5 ANT PHASESHIFT	
RF50S	RF 50S	50 RF CLEAR	50 B8 ANT PHASESHIFT	37
RF50S	RF 50S	50 RF CLEAR	50 B7 ANT	36 40
RF50S	RF 50S	50 RF CLEAR	50 B7 BALUN IN RX	
RF50S	RF 50S	50 RF CLEAR	50 B7 DPLX ANT	36
RF50S	RF 50S	50 RF CLEAR	50 B7 DUPLX RX	32 36
RF50S	RF 50S	50 RF CLEAR	50 B7 TX PAD IN	36
RF50S	RF 50S	50 RF CLEAR	50 B7 TX SAW IN	36
RF50S	RF 50S	50 RF CLEAR	50 B7 TX SAW OUT	36
RF50S	RF 50S	50 RF CLEAR	50 XCVR B7 TX	30 36
RF50S	RF 50S	50 RF CLEAR	50 B13 TX PAD IN	38
RF50S	RF 50S	50 RF CLEAR	50 B17 TX PAD IN	38
RF50S	RF 50S	50 RF CLEAR	50 B13 DPLX ANT	38
RF50S	RF 50S	50 RF CLEAR	50 B17 DPLX ANT	38
RF50S	RF 50S	50 RF CLEAR	50 B13 LPF IN	36 40
RF50S	RF 50S	50 RF CLEAR	50 B13 ANT	36 40
RF50S	RF 50S	50 RF CLEAR	50 B17 ANT	38 40
RF50S	RF 50S	50 RF CLEAR	50 B13 ANT PHASESHIFT	
RF50S	RF 50S	50 RF CLEAR	50 B17 ANT PHASESHIFT	38
RF50S	RF 50S	50 RF CLEAR	50 XCVR 2G LB TX MATCH	
RF50S	RF 50S	50 RF CLEAR	50 XCVR 2G HB TX MATCH	40
RF50S	RF 50S	50 RF CLEAR	50 2G LB PA IN	
RF50S	RF 50S	50 RF CLEAR	50 2G HB PA IN	40
RF50S	RF 50S	50 RF CLEAR	50 PRI ANT ASM	40
RF50S	RF 50S	50 RF CLEAR	50 DRX ANT TEST	41 43
RF50S	RF 50S	50 RF CLEAR	50 DRX ANT PHASESHIFT	43
RF50S	RF 50S	50 RF CLEAR	50 DRX ANT FEED	43
RF50S	RF 50S	50 RF CLEAR	50 COUPLER TERM	
RF50S	RF 50S	50 RF CLEAR	50 DIVERSITY SWITCH MATCH	41
RF50S	RF 50S	50 RF CLEAR	50 GPS INA OUT	41 42
RF50S	RF 50S	50 RF CLEAR	50 GPS ANT COAX	42
RF50S	RF 50S	50 RF CLEAR	50 GPS ANT MATCH	
RF50S	RF 50S	50 RF CLEAR	50 GPS ANT TEST	
RF50S	RF 50S	50 RF CLEAR	50 GPS INA IN	42
RF50S	RF 50S	50 RF CLEAR	50 PRI-ANT COUPLER	
RF50S	RF 50S	50 RF CLEAR	50 PRI-ANT PHASE	
RF50S	RF 50S	50 RF CLEAR	50 PRI ANT TEST	
RF50S	RF 50S	50 RF CLEAR	50 PRI ANT TEST IN	
RF50S	RF 50S	50 RF CLEAR	50 PRI ANT COAX	40 43
RF50S	RF 50S	50 RF CLEAR	50 ANT2 TERM	
RF50S	RF 50S	50 RF CLEAR	50 DRX ANT TERM	
RF60	RF 60	2G FEM S0		29 40
RF60	RF 60	2G FEM S1		25 29 40
RF60	RF 60	2G FEM S2		29 33 40
RF60	RF 60	2G FEM S3		29 33 40
RF60	RF 60	2G FEM S4		25 29 40
RF60	RF 60	2G FEM S5		29 40
RF60	RF 60	2G FEM S6		29 40
RF60	RF 60	BB PDM		29 39
RF60	RF 60	BB_PDM_FILT		39
RF60	RF 60	DCDC_ADJ		39
RF60	RF 60	PA R1		29 34 35 36 37 38

NET_TYPE		PHYSICAL	SPACING	
REF00	RF 60		WTR_GP_DATA0	29 30
REF01	RF 60		WTR_GP_DATA1	29 30
REF02	RF 60		BB_ERROR_FLAG	25 29
REF03	RF 60		PA_ON_B1_B4	29 34
REF04	RF 60		PA_ON_B2_B3	29 35
REF05	RF 60		PA_ON_B5_B8	29 37
REF06	RF 60		PA_ON_B7_B20	29 36
REF07	RF 60		PA_ON_R13_B17	29 38
REF08	RF 60		PA_BS	29 34 35 36
REF09	RF 60		LAT_SW_CTL	37 38
REF10	RF 60		PS_HOLD	25 29
REF11	RF 60		WTR_RF_ON	27 29
REF12	RF 60		WTR_RX_ON	25 29 30
REF13	RF 60		DCDC_MODE	29 39
REF14	RF 60		DCDC_ENABLE	
REF15	RF 60		DRX_ASM_V1	29 41
REF16	RF 60		DRX_ASM_V2	29 41
REF17	RF 60		DRX_ASM_V3	29 41
REF18	RF 60		DRX_ASM_V4	29 41
REF19	RF 60		19P2M_CLK_EN	27 28
REF20	RF 60		PMIC_RESOUT_L	25 27 28
REF21	RF 60		PMIC_SSBI	25 27 28

		NET_TYPE			
		PHYSICAL	SPACING		
RF	RF_DIFF	RF_DIFF	RF_60	TX_BB_Q_P	29 30
RF	RF_DIFF	RF_DIFF	RF_60	TX_BB_Q_N	29 30
RF	RF_DIFF	RF_DIFF	RF_60	DRX_BB_Q_P	29 30
RF	RF_DIFF	RF_DIFF	RF_60	DRX_BB_Q_N	29 30
RF	RF_DIFF	RF_DIFF	RF_60	GPS_BB_Q_P	29 30
RF	RF_DIFF	RF_DIFF	RF_60	GPS_BB_Q_N	29 30
RF	RF_DIFF	RF_DIFF	RF_60	PRX_BB_Q_P	29 30
RF	RF_DIFF	RF_DIFF	RF_60	PRX_BB_Q_N	29 30
RF	RF_DIFF	RF_DIFF	RF_60	DRX_BB_I_P	29 30
RF	RF_DIFF	RF_DIFF	RF_60	DRX_BB_I_N	29 30
RF	RF_DIFF	RF_DIFF	RF_60	GPS_BB_I_P	29 30
RF	RF_DIFF	RF_DIFF	RF_60	GPS_BB_I_N	29 30
RF	RF_DIFF	RF_DIFF	RF_60	PRX_BB_I_P	29 30
RF	RF_DIFF	RF_DIFF	RF_60	PRX_BB_I_N	29 30
RF	RF_DIFF	RF_DIFF	RF_60	TX_BB_I_P	29 30
RF	RF_DIFF	RF_DIFF	RF_60	TX_BB_I_N	29 30
RF	RF_DIFF	RF_100D	100_RF	100_XCVR_B13_B17_B20_PRX_P	30 33
RF	RF_DIFF	RF_100D	100_RF	100_XCVR_B13_B17_B20_PRX_N	30 33
RF	RF_DIFF	RF_100D	100_RF	100_XCVR_B8_PRX_P	30 32
RF	RF_DIFF	RF_100D	100_RF	100_XCVR_B8_PRX_N	30 32
RF	RF_DIFF	RF_100D	100_RF	100_XCVR_B5_B18_PRX_P	30 32
RF	RF_DIFF	RF_100D	100_RF	100_XCVR_B5_B18_PRX_N	30 32
RF	RF_DIFF	RF_100D	100_RF	100_XCVR_B2_B25_PRX_P	30 32
RF	RF_DIFF	RF_100D	100_RF	100_XCVR_B2_B25_PRX_N	30 32
RF	RF_DIFF	RF_100D	100_RF	100_XCVR_B3_PRX_P	30 32
RF	RF_DIFF	RF_100D	100_RF	100_XCVR_B3_PRX_N	30 32
RF	RF_DIFF	RF_100D	100_RF	100_XCVR_DCS_PCS_PRX_P	
RF	RF_DIFF	RF_100D	100_RF	100_XCVR_DCS_PCS_PRX_N	
RF	RF_DIFF	RF_100D	100_RF	100_XCVR_B1_B4_PRX_P	30 32
RF	RF_DIFF	RF_100D	100_RF	100_XCVR_B1_B4_PRX_N	30 32
RF	RF_DIFF	RF_100D	100_RF	100_XCVR_B8_B20_DRX_P	30 41
RF	RF_DIFF	RF_100D	100_RF	100_XCVR_B8_B20_DRX_N	30 41
RF	RF_DIFF	RF_100D	100_RF	100_XCVR_B5_B18_B13_B17_DRX_P	30 41
RF	RF_DIFF	RF_100D	100_RF	100_XCVR_B5_B18_B13_B17_DRX_N	30 41
RF	RF_DIFF	RF_100D	100_RF	100_XCVR_B2_B25_B3_DRX_P	30 41
RF	RF_DIFF	RF_100D	100_RF	100_XCVR_B2_B25_B3_DRX_N	30 41
RF	RF_DIFF	RF_100D	100_RF	100_XCVR_B1_B4_DRX_P	30 41
RF	RF_DIFF	RF_100D	100_RF	100_XCVR_B1_B4_DRX_N	30 41
RF	RF_DIFF	RF_100D	100_RF	100_XCVR_GPS_RX_P	30 41
RF	RF_DIFF	RF_100D	100_RF	100_XCVR_GPS_RX_N	30 41
RF	RF_DIFF	RF_100D	100_RF	100_B13_DUPLEX_RX_P	33 38
RF	RF_DIFF	RF_100D	100_RF	100_B13_DUPLEX_RX_N	33 38
RF	RF_DIFF	RF_100D	100_RF	100_B17_DUPLEX_RX_P	33 38
RF	RF_DIFF	RF_100D	100_RF	100_B17_DUPLEX_RX_N	33 38
RF	RF_DIFF	RF_100D	100_RF	100_B20_DUPLEX_RX_P	33 36
RF	RF_DIFF	RF_100D	100_RF	100_B20_DUPLEX_RX_N	33 36
RF	RF_DIFF	RF_100D	100_RF	100_DCS_PCS_RX_FILTER_P	
RF	RF_DIFF	RF_100D	100_RF	100_DCS_PCS_RX_FILTER_N	
RF	RF_DIFF	RF_100D	100_RF	100_B1_B4_DUPLEX_RX_P	32 34
RF	RF_DIFF	RF_100D	100_RF	100_B1_B4_DUPLEX_RX_N	32 34
RF	RF_DIFF	RF_100D	100_RF	100_B8_DUPLEX_RX_P	32 37
RF	RF_DIFF	RF_100D	100_RF	100_B8_DUPLEX_RX_N	32 37
RF	RF_DIFF	RF_100D	100_RF	100_B5_B18_DUPLEX_RX_P	32 37
RF	RF_DIFF	RF_100D	100_RF	100_B5_B18_DUPLEX_RX_N	32 37
RF	RF_DIFF	RF_100D	100_RF	100_B7_PRX_BALUN_OUT_P	32
RF	RF_DIFF	RF_100D	100_RF	100_B7_PRX_BALUN_OUT_N	32
RF	RF_DIFF	RF_100D	100_RF	100_B7_PRX_MATCH_P	32
RF	RF_DIFF	RF_100D	100_RF	100_B7_PRX_MATCH_N	32
RF	RF_DIFF	RF_100D	100_RF	100_XCVR_B7_PRX_P	30 32
RF	RF_DIFF	RF_100D	100_RF	100_XCVR_B7_PRX_N	30 32
			RF_CLK	SLEEP_CLK_32K	25 27 28
			RF_CLK	19P2M_WTR	27 30
			RF_CLK	19P2M_MDM	25 27 28

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
50_RF_SPACING	TOP,BOTTOM	0.178 MM	?	GND	50_RF	*	50_RF_CLEAR_SPACING
50_RF_SPACING	ISL3	0.130 MM	?	GND	50_RF_CLEAR	*	50_RF_CLEAR_SPACING
50_RF_SPACING	*	0.092 MM	?	GND	100_RF	*	100_RF_CLEAR_SPACING
50_RF_CLEAR_SPACING	TOP,BOTTOM	0.178 MM	?	GND	RF_60	*	1.2:1_SPACING
50_RF_CLEAR_SPACING	ISL3	0.130 MM	?	GND	PWR_RF	*	1.2:1_SPACING
50_RF_CLEAR_SPACING	*	0.138 MM	?	PWR_RF	PWR_RF	*	1.2:1_SPACING
100_RF_CLEAR_SPACING	TOP,BOTTOM	0.143 MM	?	RF_CLK	*	*	3:1_SPACING
100_RF_CLEAR_SPACING	*	0.118 MM	?	RF_CLK	GND	*	1.2:1_SPACING

```
NC PMU OUT 32K CLK GPS — PMU OUT 32K CLK GPS IN 57
NO_TEST=TRUE 64
MAKE_BASE=TRUE
```

